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VOL. 7 No. 62 JANUARY 1963

Mullard Technical Communications

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Mullard

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Published by

Technical Information Department
Mullard Limited, Mullard House, Torrington Place, London, W.C.1
LANgham 6633

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Made and Printed in England by
WIGHTMAN AND COMPANY LIMITED, 1/3 BRIXTON ROAD, LONDON, S.W.9

Anode Circuit Design for the Z806W in Relay Operation

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The Mullard Z806W trigger tube is specially designed for mains operation. Graphs in this article indicate the values of resistance for the anode circuit with a wide range of relay characteristics.

INTRODUCTION

The anode circuit of a trigger tube which is controlling a relay must fulfil certain requirements if the circuit is to operate satisfactorily. These requirements are explained in this article, and used to derive precise information concerning the anode circuit of the Z806W trigger tube. The graphs at the end of the article enable the Z806W anode circuit to be designed easily and in a way that allows for mains voltage variation and other variables.

The characteristics of the Z806W trigger tube make it suitable for operation directly from mains supply with relays; its highly stable trigger ignition voltage also makes its use advantageous in many control circuits. There is a screening anode between the anode and the cathode and this screen is held at a positive voltage during periods when the tube is expected to conduct.

The tube has been designed for use with the range of mains voltage likely to be encountered; that is, nominally 200V to 250V with a variation of ±10%. For the tube and relay to be able to work over this wide range of supply voltage in the simple circuit shown in Fig. 1, the main requirement to be met by the circuit is that the limiting resistance in the anode circuit must be high enough to safeguard the tube and yet low enough to allow the relay to operate reliably.

The information provided in this article facilitates the design of anode circuits for the Z806W tube by indicating suitable values for the total anode series resistance with each value of relay resistance and pull-in current. The values of resistance are valid for the circuit shown (Figs. 1 and 3) and can be easily modified, in the way referred to below, for the similar circuits using full-wave rectification of the supply voltage.

CIRCUITS

A typical relay operation circuit is shown in Fig. 1. In this application the control voltage is fed directly to the trigger circuit so that when the trigger ignition voltage is reached the anode can ignite on each positive half cycle. Rectified mains must be used since negative voltages on the anode are not permissible. The anode and screen are therefore extinguished regularly and stay extinguished if the control voltage falls below the trigger ignition voltage. The trigger circuit is also arranged to ignite and extinguish regularly at a suitably higher frequency than the mains, and the capacitance used ensures reliable transfer of discharge even with a high-impedance control-voltage supply.

Screen Circuit

The arrangement suggested for the resistors of the screen circuit is to be found in the published data for the Z806W. The full range of mains voltage, that is 200V to 250V nominal ±10%, is covered by two settings of the potential divider network. The supply impedance to the screen must be about 120kΩ and the attenuation ratio should be 76·5% for the 200V to 230V nominal range, and 67·5% for the 230V to 250V nominal range. The values of the resistors in Fig. 1 are 33kΩ for R_2 and 100kΩ for R_4. If the mains voltage is in the upper range then R_3 should be 68kΩ, or if in the lower range then R_3 should be 68kΩ plus 39kΩ. Other screen circuits can be designed.

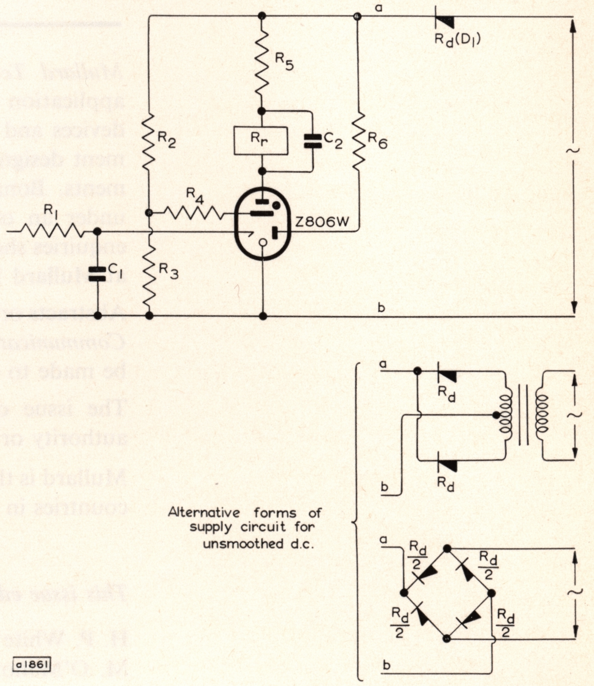

Fig. 1—Circuit for relay operation directly from a.c. mains

Trigger Circuit

The trigger circuit shown in Fig. 1 is a self-extinguishing circuit. The frequency of trigger ignition affects the point in the mains cycle at which anode ignition occurs: high frequency trigger ignition will always ensure anode ignition early in a positive half-cycle, while a lower frequency may allow anode ignition later than the mains peak, or may even fail to give ignition. Early anode ignition gives a high mean current for a given peak current, and so ignition before the peak is preferable. Only when the anode has reached its minimum working voltage, however, can trigger ignition cause the anode to ignite; this voltage corresponds to approximately 60° in the a.c. mains cycle at 180V. The trigger must, therefore, ignite repeatedly at intervals of rather less than 30° of the mains cycle to guarantee ignition on each positive half cycle before the 90° point (Fig. 2). A time-constant in the trigger circuit of 300 to 500μs amply satisfies this condition. Since a 1nF capacitor is recommended in the data to ensure good transfer of discharge, the effective resistance in the trigger circuit should be 500kΩ. This value is the sum of the source resistance and the value of R_1 in Fig. 1. The half sine-waves of Figs. 2a to 2f indicate the variations which bring about the two limit conditions of Fig. 2g and 2h. Here V_m is the maintaining voltage of the tube and V_r the voltage across the relay.

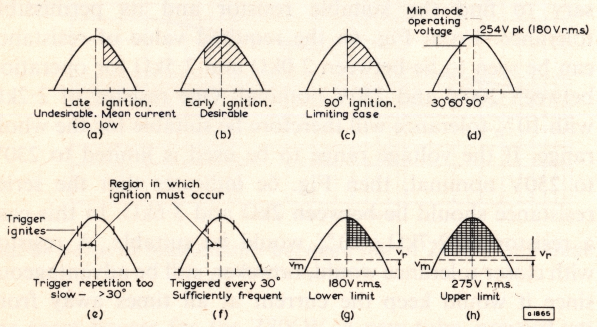
Min anode operating voltage
254V pk (180Vr.m.s)
Late ignition. Undesirable. Mean current too low
(a)
Early ignition. Desirable
(b)
90° ignition. Limiting case
(c)
30°60°90°
(d)
Region in which ignition must occur
Trigger ignites
Trigger repetition too slow – >30°
(e)
Triggered every 30° Sufficiently frequent
(f)
Vm
Vr
180V r.m.s. Lower limit
(g)
Vm
Vr
275V r.m.s. Upper limit
(h)
a1865

Fig. 2—Various ignition conditions leading to maximum and minimum anode current

The least advantageous but usable ignition frequency is assumed in the calculation of maximum values of series anode resistance, given below in the various graphs. In some applications the supply to the trigger may be capable of giving a higher ignition frequency. Under such conditions the value of series resistance may be increased slightly without the relay failing to pull in.

Anode Circuit

The most simple and inexpensive circuit for relay operation uses a single rectifier diode connected directly to the mains. The values of limiting resistance in the anode circuit shown in the graphs on pages 42 to 47 are valid for such a circuit in which half-wave rectification occurs. In some circuits the benefits of a four-diode bridge, or a transformer and two diodes, to give full-wave rectification, may be deemed sufficient to justify their use, particularly when the transformer is to be present in any case for other reasons.

The values of series resistance indicated in the graphs are for half-wave rectification: if full-wave rectification is to be used then the value should simply be doubled, provided that any serious differences in the values of rectifier resistance are taken into account.

The 'pulsed' current supplied by the trigger tube may cause relay chatter. This is avoided by adding the capacitor C_2 in parallel with the relay, as shown in Fig. 1. The time-constant of the relay and capacitor together should be at least 30 to 50ms. In addition to the capacitor, a further resistor is required in series with the relay to limit the current through the tube. This limiting is mainly on the peak currents which can pass through the low impedance of the capacitor. The total series resistance (R_s) in the main circuit is then the sum of the resistance of the rectifier diode (R_d), and the extra resistance (R_5). The resistance R_d, the forward resistance of the diode, is likely to be less than 100Ω and usually less than 10Ω and so can be ignored. Therefore R_s can normally be taken to be equal to the value of R_5.

When using relays with a resistance of 4kΩ or more in the circuit of Fig. 1 there is a possibility that the voltage developed across the relay capacitor might exceed 90V. The anode voltage would then be taken beyond its maximum negative limit during the period that the diode is cut off. To prevent this a further diode D_2 should be introduced in series with R_5 (see Fig. 3), and a high resistance R_7 connected between the anode and the h.t. line. An OA202 with a parallel resistor of 1MΩ may be used, and a 470kΩ resistor from the h.t. line to the anode, as shown in Fig. 3.

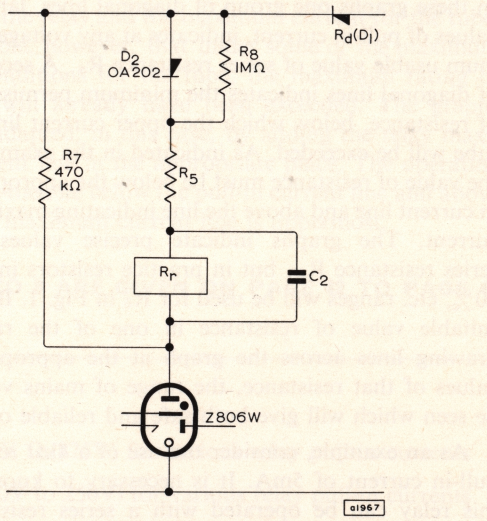

Fig. 3—Alternative circuit for use with relays of resistance of 4kΩ or more

The minimum current under adverse conditions must still be capable of pulling in the relay. The worst conditions occur when the mains voltage is at 200V−10%, or 180V, and the trigger is igniting only at about the peak in the mains cycle. This may take place if the trigger fails to transfer the discharge on its ignition just before the 60° point and the igniting frequency is such as to give trigger ignition only about every 30° of the mains cycle (Fig. 2g). The maximum value of the total series resistance R_s is governed, therefore, by this minimum average current under worst conditions.

The maximum current for which allowance must be made occurs when the mains voltage has risen to 250V+10%, or 275V, and the trigger ignites the main discharge regularly as soon as the anode reaches its transfer voltage (Fig. 2h). The limiting value of current for the tube must not be exceeded under these conditions.

CALCULATIONS

The information in the graphs is derived by integrating the appropriate areas (shaded) in Figs. 2g and 2h and averaging over one cycle to give the mean voltage across R_s. The value of R_s is obtained by dividing this mean voltage by the mean current (the pull-in current) appropriate to the value of relay resistance. Similarly, the value of the peak current is obtained from R_s and the peak voltage across R_s. Throughout the calculations it was assumed that the voltage across the relay, V_r, was held constant by the capacitor C_2. The voltage V_r equals the mean current multiplied by the relay resistance.

INTERPRETATION OF GRAPHS

The value of total series resistance (R_s) under each set of voltage conditions and for each value of relay pull-in current may be obtained from Figs. 4a to 4f (page 42), each graph being for a separate value of relay resistance. In these graphs one group of diagonal lines, labelled with values of pull-in current, indicates at any voltage the maximum usable value of series resistance R_s. A second group of diagonal lines indicates the minimum permissible value of resistance, below which the upper current limits of the tube will be exceeded. As indicated in the example below, the value of resistance must be below the appropriate pull-in current line and above the line indicating maximum tube current. The graphs indicate precise values of total series resistance R_s, but in practice resistors in the 20%, 10%, etc. ranges will be used for R_5 in Fig. 1. By taking a suitable value of resistance in one of the ranges and drawing lines across the graph at the appropriate limit values of that resistance, the range of mains voltage can be seen which will give both safe and reliable operation.

As an example, consider the use of a 4kΩ relay with a pull-in current of 5mA. It is necessary to know whether this relay can be operated with a series resistor in the 10% tolerance range, and what value the resistor should be for 230V. Using the 100mA limit on the graph applicable to a 4kΩ relay (Fig. 4c) it can be seen that at 230V the value of the extra series resistance must lie between 1·4kΩ and 4·5kΩ for operation to be both safe and reliable. An ideal value of resistance allowing the widest voltage variation is 2·25kΩ. The extreme values of 2·2kΩ, which is a preferred value resistor in the 10% range, are 2·0kΩ and 2·4kΩ and the limiting voltages can be seen to be 177V and 275V. In this particular case, therefore, the one 10% resistor allows operation over the complete voltage range considered. The use of the 200mA peak and 25mA mean limits is discussed later.

The information given in Figs. 4a to 4f is repeated with one modification in Fig. 5a to 5f. The voltages on the abscissae of Fig. 5 are nominal voltages and so the resistance curves allow for ±10% voltage variation.

To facilitate selection of series resistors with various relays, Figs. 6a, 6b and 6c show directly the series resistance against relay resistance. These and subsequent curves are derived directly from Fig. 5. The curves of Fig. 6a are for the complete range of 200V to 250V nominal, and the curves of Fig. 6b and 6c are for the two ranges corresponding to the screen supply voltage, 200V to 230V nominal (Fig. 6b) and 230V to 250V nominal (Fig. 6c). Again, the value of resistance used must fall below the pull-in current line and above the tube limit lines.

In Fig. 6 full allowance is made for the possible variation of 10% from the nominal mains voltage. The pull-in current lines are therefore plotted for the −10% condition in each case, that is 180V for 200V nominal and 207V for 230V nominal. The overload lines for the tube are drawn for the +10% condition, 253V for 230V nominal and 275V for 250V nominal.

Taking as an example the conditions used previously, namely a 4kΩ relay with a 5mA pull-in current, it is necessary to find the suitable resistor and its permissible tolerance. From Fig. 6a the required value of resistance can be seen to lie between 2·0kΩ and 2·5kΩ for operation between 200V and 250V nominal. One resistor of 2·2kΩ with 10% tolerance will therefore be suitable for the whole range. If the voltage range to be used is limited to 230V to 250V nominal, then Fig. 6c indicates that the series resistance should lie between 2kΩ and 3·6kΩ. In this case a resistor of 2·7kΩ±20% would be suitable. A resistor with closer tolerance would, however, still be advantageous since it would keep the current at all times away from the limits.

Figs. 7a to 7f give the same information in such a way as to assist in the rapid design of circuits. The curves of Figs. 7a and 7b indicate the limits of usable combinations of relay resistance and pull-in current, over the voltage ranges specified: only values of pull-in current below the limit lines are satisfactory. Fig. 7c and 7d show the optimum value of series resistance and its tolerance ($R_s$tol). If the point used on the curve is below the 20% tolerance line, then 20% tolerance is sufficient: linear interpolation of the tolerance curves is permissible. If the two separate ranges of voltage are to be used, the relevant information is given in Figs. 7e and 7f : both of these describe conditions for the range 200V to 230V nominal, but both can be adapted to the range 230V to 250V nominal by adding 0·5kΩ to the values of series resistance obtained.

Consider once again, as an example, the 4kΩ relay with 5mA pull-in current. Fig. 7a shows that such an arrangement is possible over all the range of voltage since the point corresponding to 4kΩ and 5mA is below all the limit lines. Fig. 7d indicates that the ideal series resistance is 2·25kΩ at a tolerance of approximately 10%. For operation in only the 230V to 250V range, Fig. 7e (adding 0·5kΩ) gives the value as 2·6kΩ at 20% tolerance.

Where full-wave rectification is used in the circuit the values of series resistance obtained from Fig. 7 and previous graphs should be doubled, since they are for half-wave rectification. If the curves are treated in this way for full-wave rectification then the 200mA peak referred to becomes 100mA peak, the 25mA mean remaining unaltered.

As an example, however, Fig. 8 gives directly, for full-wave rectified supplies, the information previously given for half-wave rectification in Fig. 7c.

CHOICE OF LIMITING CURRENT

The limiting conditions for the Z806W have been taken in this article as 25mA mean and 200mA peak. The 25mA mean current rating given in the data is intended to prevent the dissipation of too much power in the tube, and should not under any circumstances be exceeded.

The value of peak current, however, has a great effect on the useful life of the tube used in a circuit of the kind described, where the supply is a sinusoidal alternating current. The usual relationship, of the form shown in Fig. 9, between useful life and peak current can be expected to exist: since full information on this topic depends on life-tests of many tubes over periods exceeding 30,000 hours, the exact figures for the Z806W, a new tube, are not yet available. The indications are that the useful life of the Z806W will exceed 1000 hours at 200mA peak current, and 14,000 at 100mA peak current.

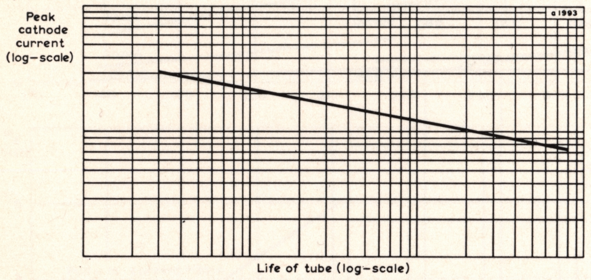

Fig. 9—Form of relationship between life of Z806W and peak cathode current

When evaluating the maximum peak current likely to occur in operation, the designer should remember that this maximum will occur only when the mains input voltage is at the top limit with the highest nominal voltage, that is, 275V on 250V nominal. This is likely to occur only for a small percentage of the time that the relay is energised, probably between 1% and 5%. This fact, combined with a low duty cycle of the relay will indicate that high values of total useful life may be obtained in this kind of circuit with the Z806W.

In the first few cycles of any conduction period, while a voltage is building up across the relay, the peak currents will be much higher than usual, and this must be taken into account if only very short conduction periods are used.

RELAYS

From the various graphs it can be seen that the pull-in current of relays used with the Z806W tube over the full voltage range, is limited to about 6mA if half-wave rectification is employed. With full-wave rectification, and also with half-wave if a 200mA peak limit is used, the maximum usable current rises to about 12mA in the region of 7kΩ and 8kΩ relays. If the supply voltage is limited to one nominal value, then an extra current of 1mA to 3mA can be obtained, still observing the 100mA peak maximum.

In all the above considerations the working range of the circuit has been limited only by the minimum pull-in current of the relay and the maximum current for the tube. It is possible, however, that under some of the maximum current conditions for the tube, the maximum rating of the relay will already have been exceeded. The graphs could be adapted, in this case, by adding the relay maximum current line in the appropriate place. The operating conditions then lie below the pull-in current line and above whichever maximum current line is uppermost.

FIGS. 4 TO 8 ARE GIVEN ON PAGE 42 TO PAGE 47

LIST OF GRAPHS

Fig. 4—Series resistance (R_S) plotted against mains supply voltage (180V to 275V) for various relay pull-in currents
Fig. 5—Series resistance (R_S) plotted against nominal mains voltage (200V to 250V) for various relay pull-in currents
Fig. 6—Series resistance (R_S) plotted against relay resistance (R_T) for various pull-in currents,
Fig. 6a—for 200V to 250V
Fig. 6b—for 200V to 230V
Fig. 6c—for 230V to 250V
Fig. 7—Pull-in current plotted against relay resistance (R_T),
Fig 7a—for 200V to 250V
Fig. 7b—for either 200V to 230V or 230V to 250V
Pull-in current plotted against series resistance (R_S),
Fig. 7c—for 200V to 250V, 25mA mean current
Fig. 7d—for 200V to 250V, 100mA peak current
Fig. 7e—for 200V to 230V, 25mA mean current
Fig. 7f—for 200V to 230V, 100mA peak current
(N.B.—Figs. 7e and 7f can be adapted for 230V to 250V operation)
Fig. 8—Pull-in current plotted against series resistance (R_S) for full-wave rectified supply (200V to 250V)

Figs. 4(a to f)—Limiting values of R_s plotted against mains supply voltage

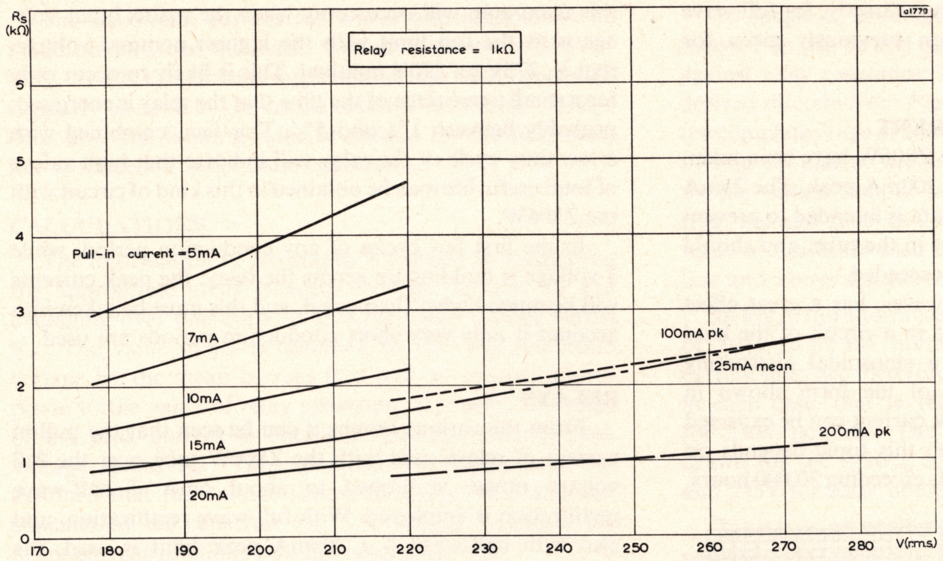

Fig. 4a

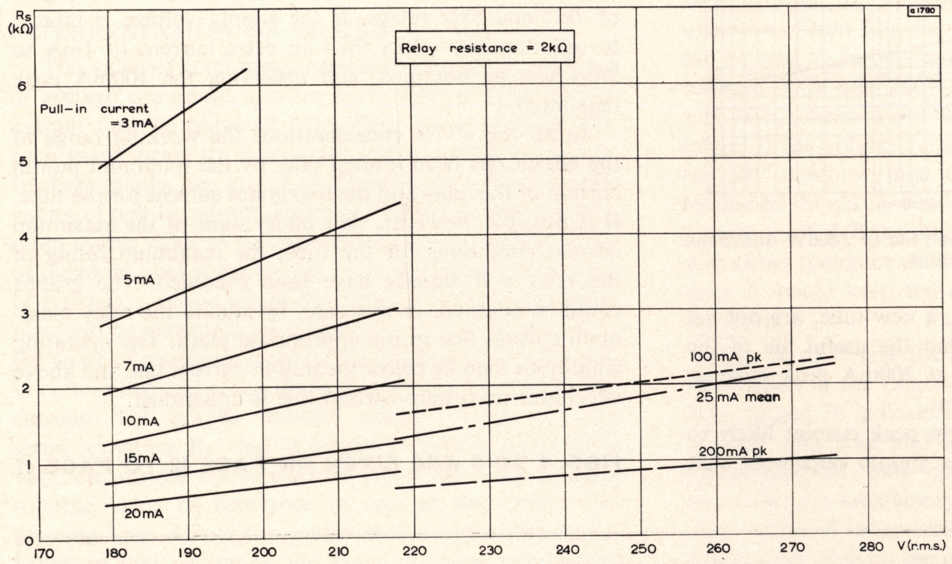

Fig. 4b

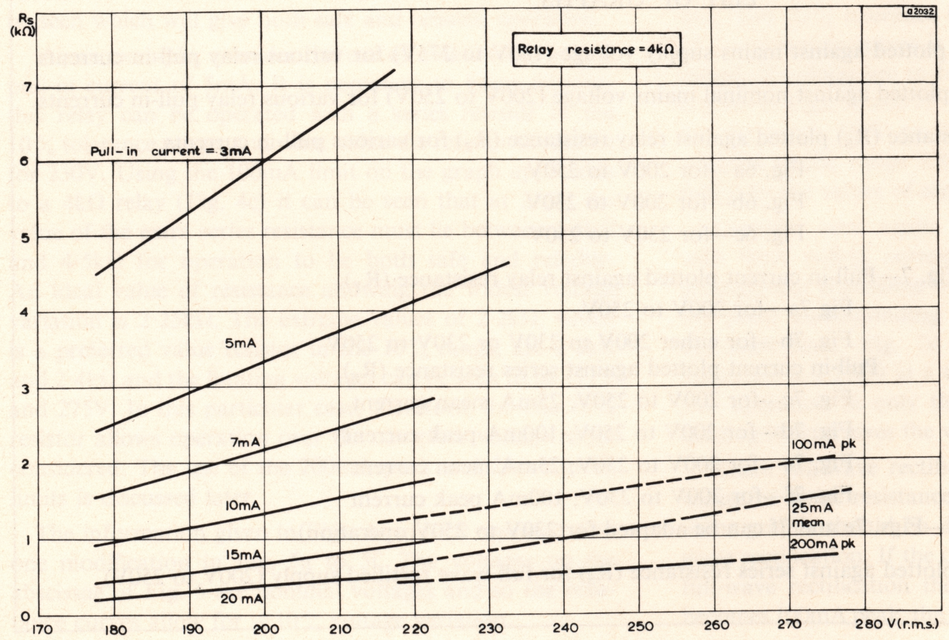

Fig. 4c

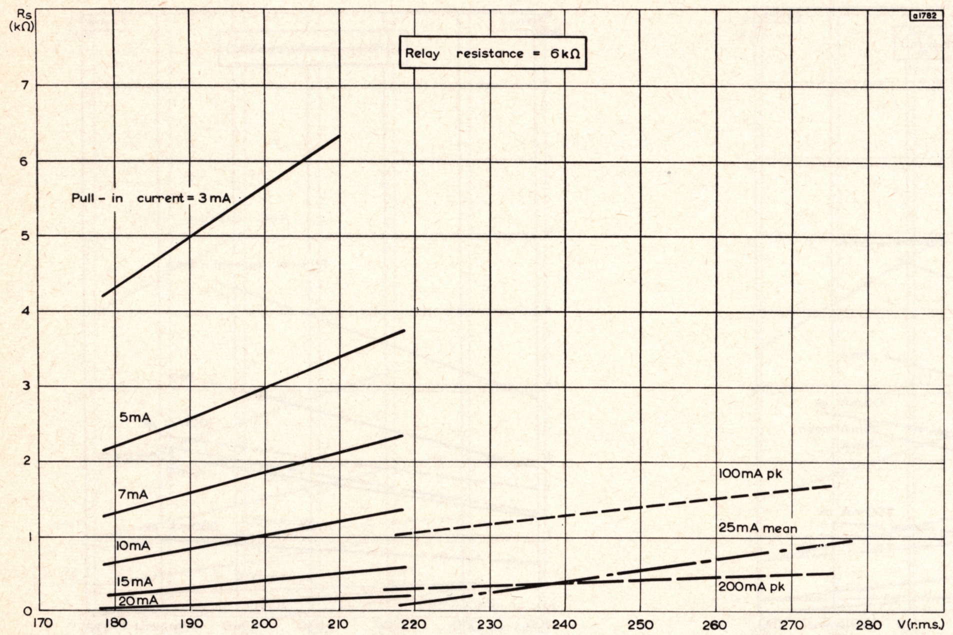

Fig. 4d

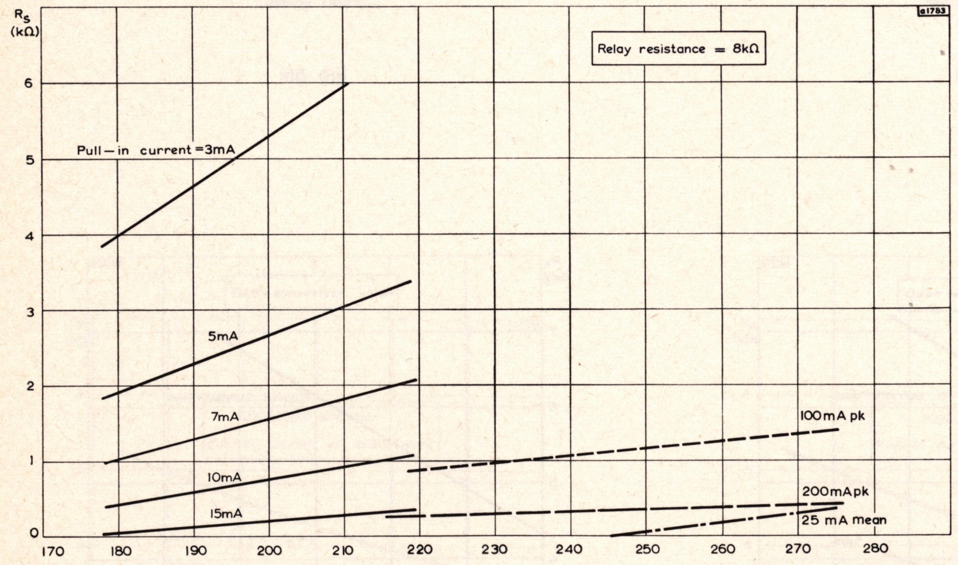

Fig. 4e

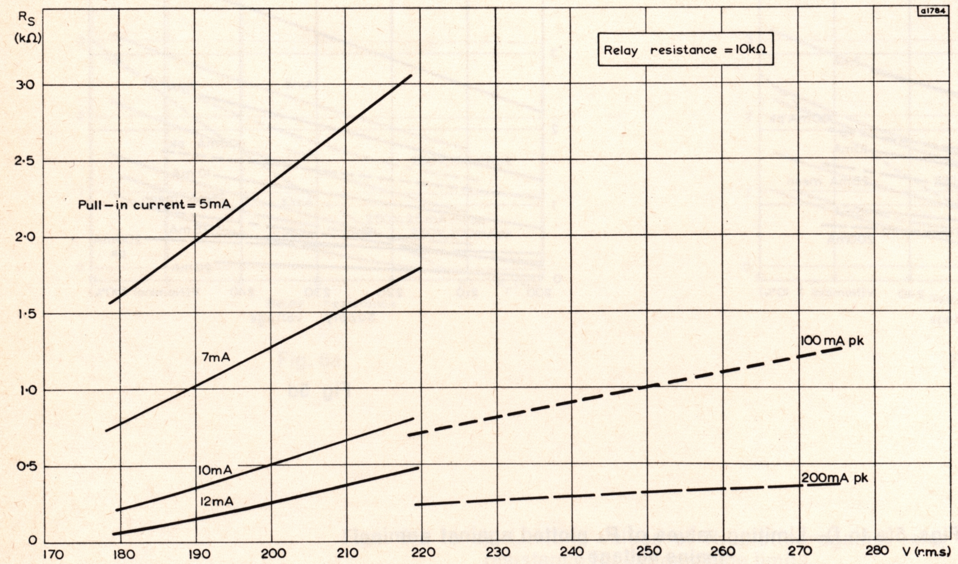

Fig. 4f

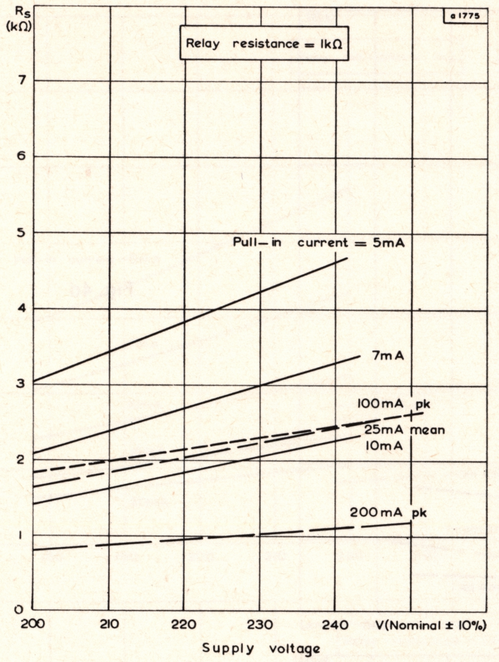

Fig. 5a

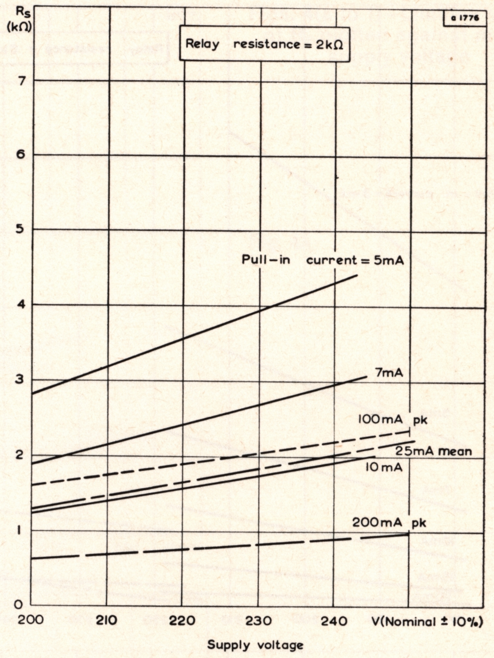

Fig. 5b

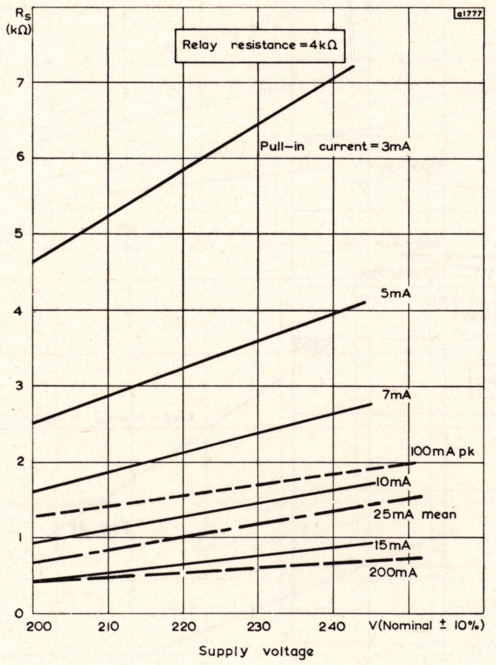

Fig. 5c

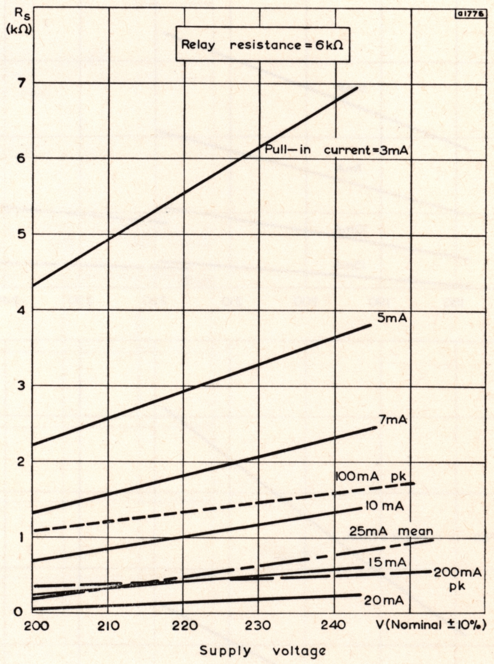

Fig 5d

Figs. 5(a to f)—Limiting values of R_s plotted against nominal mains voltage

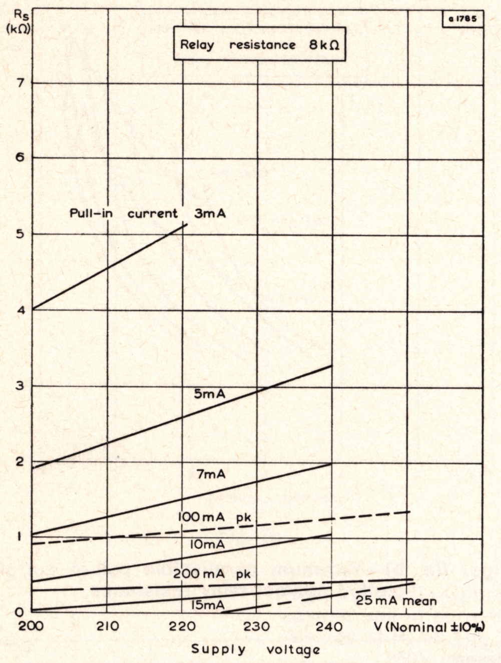

Fig. 5e

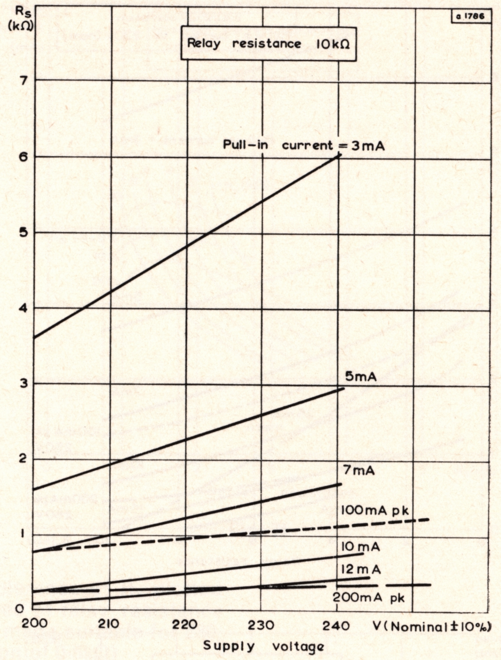

Fig. 5f

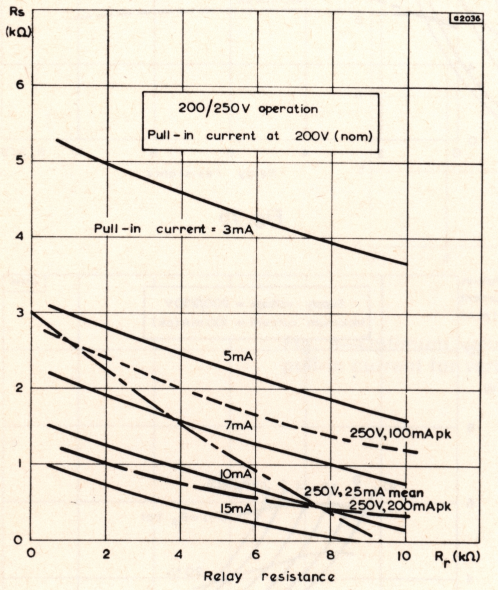

Fig. 6a

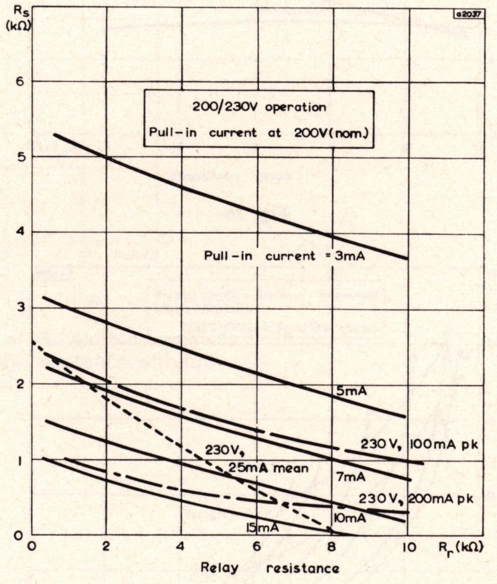

Fig. 6b

Figs. 6(a to c)—Limiting values of R_s plotted against relay resistance for various tube limits

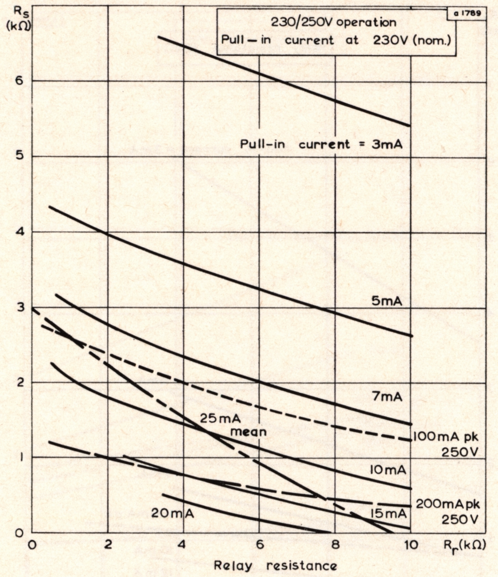

Fig. 6c

Figs. 7(a, b)—Maximum permissible pull-in current plotted against relay resistance

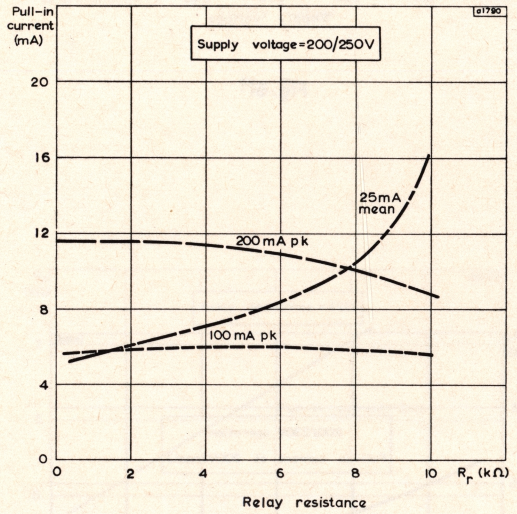

Fig. 7a

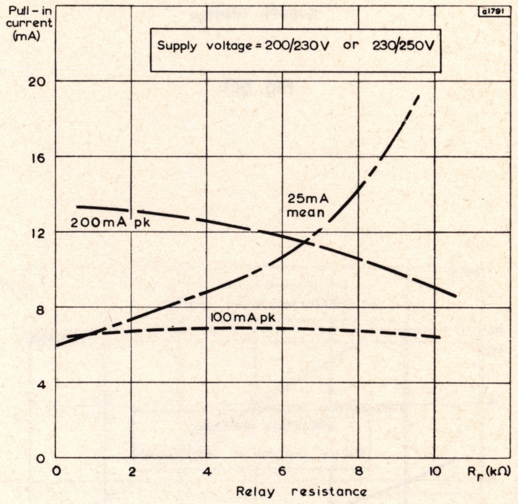

Fig. 7b

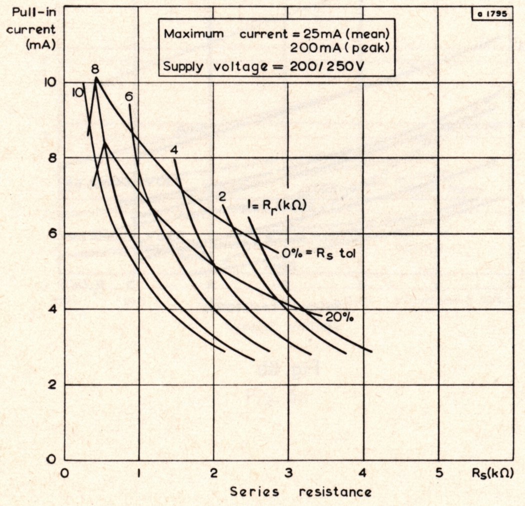

Fig. 7c

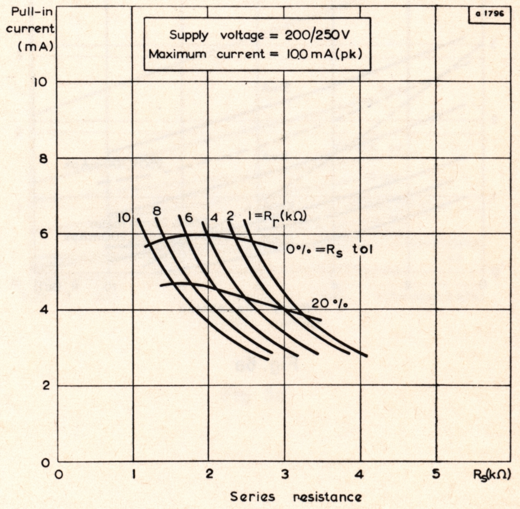

Fig. 7d

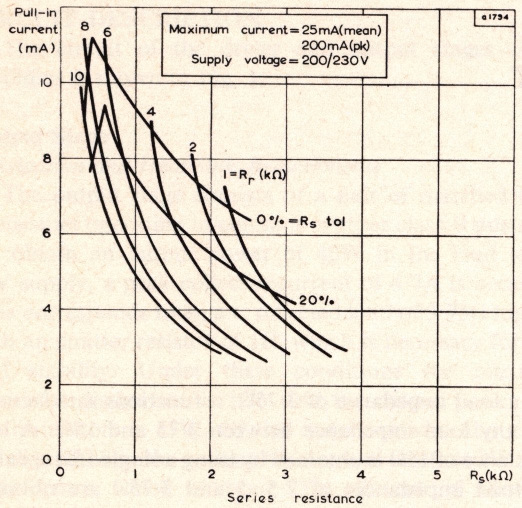

Fig. 7e

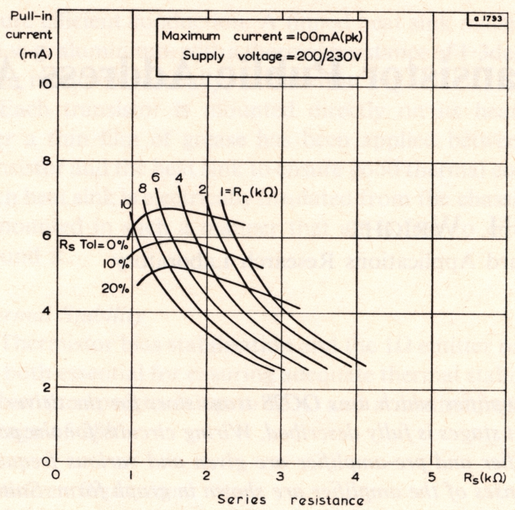

Fig. 7f

Figs. 7(c to f)—Optimum value and tolerance of R_s plotted against pull-in current for various values of relay resistance (Values of R_s on Fig. 7e and 7f can be made suitable for 230/250V operation by the addition of 0·5kΩ)

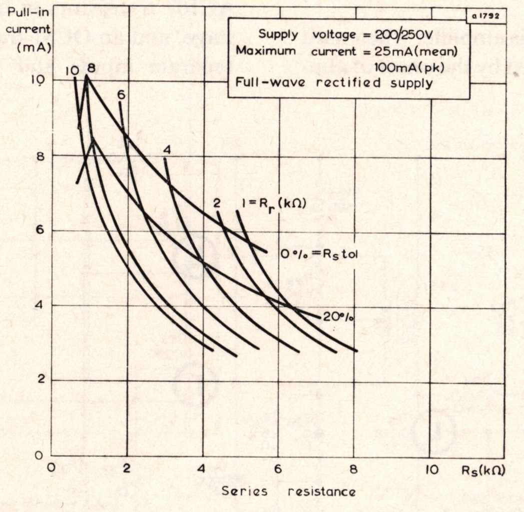

Fig. 8—Optimum value and tolerance of R_s plotted against pull-in current for various values of relay resistance with full-wave rectified supply

Transistor Public Address Amplifier

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An amplifier which uses OC28 transistors for the driver and output stages is fully described. Wiring circuits for the power amplifier and pre-amplifier are given and various frequency responses of the amplifier are shown in graph form. Suitable designs for the heat sinks are also provided.

The performance of the amplifier easily meets the requirements of public address systems and the amplifier may be used with most low-impedance microphones and crystal pick-ups.

INTRODUCTION

The circuit diagram for a 40W, 24V public address amplifier is given in Fig. 1.

The maximum output power of this amplifier when used with a 3·75Ω load impedance is limited by the onset of clipping to 40W, and the low and high −3dB cut-off frequencies at this output power are 120c/s and 18kc/s respectively. Distortion is 2·3% at 40W output power and is considerably less at lower output powers (distortion is 10% at 48W output power). Input sensitivities are such that the amplifier (plus pre-amplifier) may be used with most low-impedance microphones and crystal pick-up heads.

Although the amplifier is primarily designed for use with a load impedance of 3·75Ω, it functions satisfactorily with any load impedance between 3·75 and 15Ω. A load impedance of 15Ω is obtained by using a single 15Ω speaker, and load impedances of 7·5, 5 and 3·75Ω are obtained by using two, three or four 15Ω speakers respectively, in parallel.

Output is provided by a matched pair of OC28 transistors operating in a common-emitter class B push-pull amplifier, and the drive current for the output pair is obtained from an OC28 transistor which operates under class A conditions. The driver stage is preceded by amplifying stages (which are given in Fig. 9) incorporating AC107 transistors in both the input stages and the second stage, and an OC81 transistor in the third stage. There are separate inputs and volume controls provided for the low-impedance microphone and the crystal pick-up head; it is possible to mix these inputs.

Continuous operation of the amplifier at an ambient temperature of 45°C is possible: the unit is thermally stable up to 55°C.

The amplifier can be made quite compact even though a heat sink of thermal resistance as low as 1·3degC/W is necessary for each output transistor.

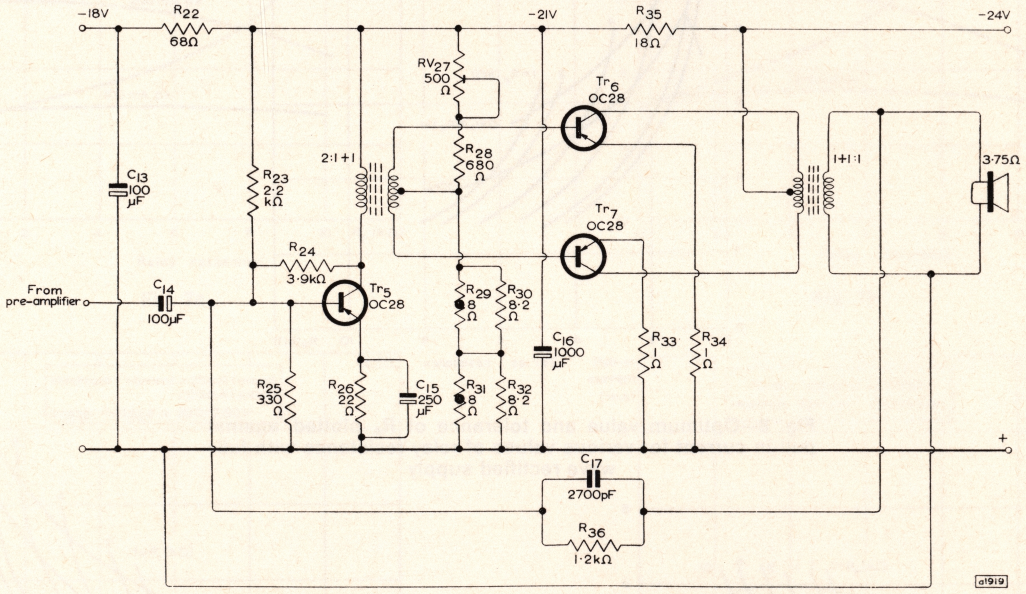


Fig. 1—Circuit diagram for 40W, 24V public address amplifier

CIRCUIT DESCRIPTION

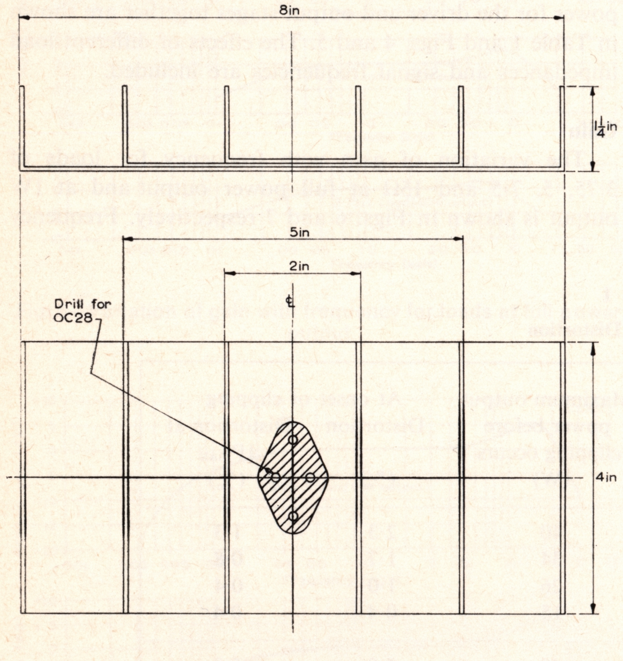
The circuit of the driver and output stages of the amplifier is shown in Fig. 1.

Output Stage

Dissipation and Heat-sink Requirements

The output stage consists of a pair of matched OC28 transistors operating in common-emitter class B push-pull. To obtain an output power of 40W in the load with a 24V supply, a peak collector current of 4·7A is necessary. This corresponds to an a.c. reflected load of 3·75Ω together with an emitter resistor of 1Ω, which is necessary for thermal stability. Under these conditions the maximum transistor dissipation is 12W and the output power from the transistors is 53W. Of this output power, about 11W are dissipated in the emitter resistor and another 2W in the transformer, which is about 95% efficient. If allowance is made for an increase of the supply voltage to 28V, the maximum transistor dissipation will be increased to 16·3W and the output power from the transistors will also be increased.

At a supply voltage of 28V and an ambient temperature of 45°C, a transistor junction temperature of 90°C will be attained with a heat sink having a thermal resistance of 2·8degC/W. As the thermal resistance between the transistor junction and the mounting base is 1·5degC/W, the required thermal resistance between the heat sink and ambient is 1·3degC/W. Therefore the heat sink should be compact in design and have a thermal resistance of 1·3degC/W. For efficient cooling of the transistor the heat sink should have a large blackened surface area and the metal under the transistor should be thick enough to ensure efficient conduction. A finned heat sink made from 16s.w.g. aluminium, with a thermal resistance of 1·3degC/W when mounted vertically, is shown in Fig. 2.



Finish: matt black except under transistor (shaded area)

θ = 1·3 deg C/W Material 16s.w.g. aluminium

Fig. 2—Heat sink for each output transistor

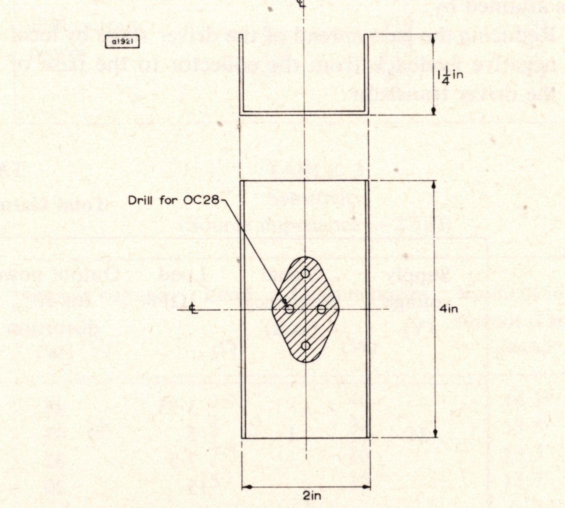
Each transistor is mounted directly on its heat sink after a thin film of grease has been applied between the transistor and the heat sink to ensure good thermal contact. Each heat sink is electrically insulated from the chassis and is mounted in such a manner that air is free to circulate around it.

Thermal Stability

Thermistor bias stabilisation and the 1Ω emitter resistor are both essential for ensuring adequate thermal stability at ambient temperatures up to 55°C and a maximum supply voltage of 28V.

Crossover Distortion

Crossover distortion is minimised by the adjustment of the preset control RV$_{27}$ to obtain a total quiescent current of 60mA for the pair of output transistors. Thermistor stabilisation of bias ensures that this optimum bias condition exists for all ambient temperatures between 0°C and 45°C.



Finish: matt black except under transistor (shaded area)

θ = 3·3 deg C/W Material 16 s.w.g. aluminium

Fig. 3—Heat sink for driver transistor

Output Transformer

This transformer has a 1+1 : 1 turns ratio to match a 3·75Ω load. The primaries are bifilar wound and each winding has a resistance of less than 0·1Ω. Each winding of the transformer used in the prototype amplifier had an inductance of 5mH. The output transformer should be capable of handling a peak current of 6A.

Driver Stage

The driver stage consists of an OC28 transistor operating under class A conditions and the driver collector current is 120mA. As the maximum dissipation of the driver transistor is 2W, a relatively small heat sink may be used. Fig. 3 shows the heat sink used in the prototype amplifier and this particular heat sink has a thermal resistance of 3·3degC/W when mounted vertically.

Application of local negative feedback, from the collector to the base of the driver transistor, reduces the a.c. gain spreads of the amplifier by approximately 7dB.

The driver transformer has a turns ratio of 2 : 1+1. The primary resistance should be less than 6Ω and secondary resistances should be less than 2Ω; the secondaries are bifilar wound. The transformer used in the prototype amplifier had a primary inductance of 400mH at 150mA.

Negative Feedback

At full output with a 3·75Ω load, overall negative feedback of approximately 9dB is applied from the secondary of the output transformer, via R_{36} and C_{17}, to the base of the driver transistor.

When using a 15Ω load – the amplifier is primarily designed for use with a 3·75Ω load impedance but it functions satisfactorily with any load impedance between 3·75Ω and 15Ω – a stability margin of 6dB is required and this is attained by:

(i) Reducing the gain spread of the driver stage by local negative feedback from the collector to the base of the driver transistor.

(ii) Having a suitable capacitor C_{17} in parallel with the main feedback resistor R_{36}.

(iii) Choosing suitable values of low frequency time constants. The values chosen depend on the particular transformers being used and should be such that the phase change produced does not give rise to instability. The value of 250μF for C_{15}, in particular, was chosen for this reason.

Approximately 20dB of feedback is applied with a 15Ω load. The prototype amplifier had a stability margin of 6dB when the load was provided by a 15Ω speaker. However, the stability margin may be less with other types of single 15Ω speakers which would make it necessary to reduce the amount of overall negative feedback by switching in a higher value of feedback resistor R_{36}.

PERFORMANCE

Distortion

Variations of total harmonic distortion with load power for the driver and output stages together are shown in Table 1 and Figs. 4 and 5. The effects of different load impedances and signal frequencies are included.

Gain

The variation of gain with frequency for loads of 3·75, 5, 7·5 and 15Ω at full power output and at 1W output is shown in Figs. 6 and 7 respectively. Frequency response curves for 3·75Ω load at 1W level with or without feedback are shown in Fig. 8: and it can be seen that at this low power level the amount of overall negative feedback is 12dB over most of the audio band. Table 2 shows the −3dB cut-off frequencies with feedback for load values of 3·75, 5, 7·5 and 15Ω at both low signal strength and full output power.

Sensitivity

The sensitivity of the amplifier is given in Table 3.

TABLE 1
Total Harmonic Distortion

Supply voltage (V)	Signal frequency (kc/s)	Load (Ω)	Output power for 10% distortion (W)	Maximum output power before clipping occurs (W)	At onset of clipping Distortion (%)	Distortion at ½P_{max} (%)
24	1	3·75	48	40	2·3	1·3
		5	41	34	1·7	0·8
		7·5	32	26	1·0	0·4
		15	20	15	0·4	0·4
24	4	3·75	46	40	7·8	5·3
		5	42	34	6·6	4·1
		7·5	33	26	4·7	2·4
		15	20	15	2·1	0·9

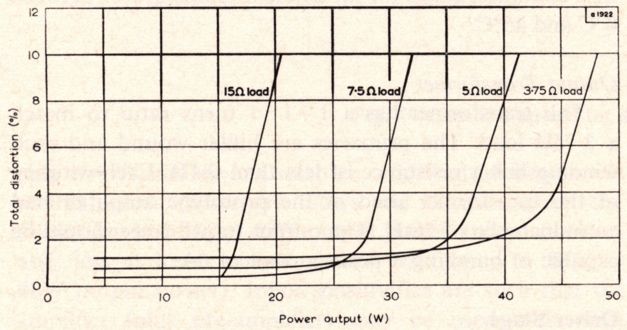


Fig. 4—Total harmonic distortion at 1kc/s (Supply voltage 24V)

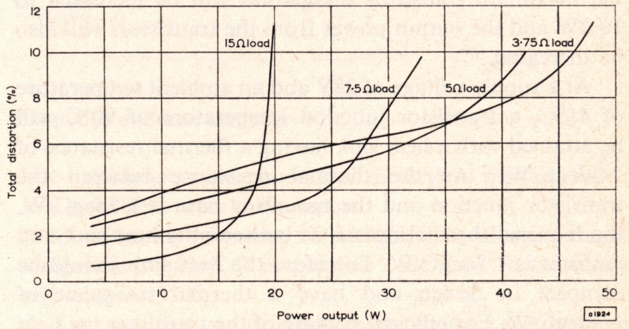


Fig. 5—Total harmonic distortion at 4kc/s (Supply voltage 24V)

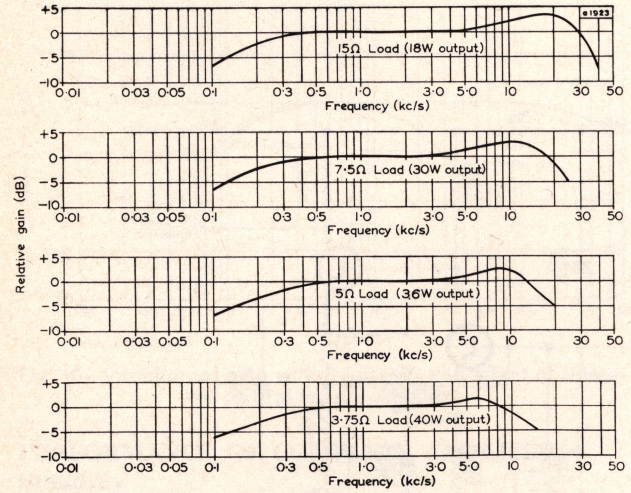


Fig. 6—Variation of gain with frequency for loads at full power output

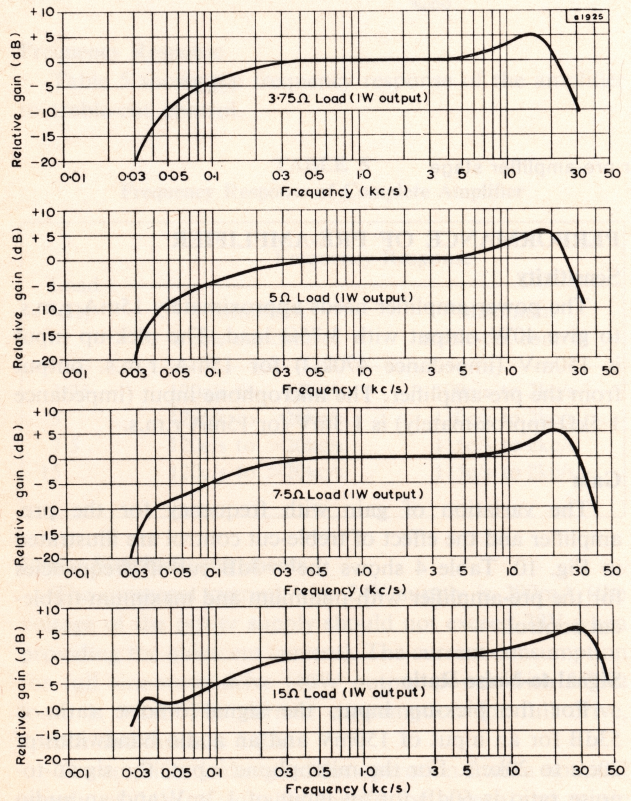


Fig. 7—Variation of gain with frequency for loads at 1W output

PRE-AMPLIFIER

Three stages of amplification (given in the circuit of Fig. 9) are necessary for the input signals from a microphone or a crystal pick-up. The pre-amplifier has separate input stages for both pick-up and microphone.

Input Stage

From dynamic range considerations it is desirable to have the volume control as early in the circuit as possible.

TABLE 2
Cut-off Frequencies

	Load (Ω)	−3dB cut-off frequency with feedback Low (c/s)	High (kc/s)
Low signal strength (1W output)	3·75	80	26
	5	80	30
	7·5	80	36
	15	80	47
Full output power	3·75	95	18
	5	110	20
	7·5	115	25
	15	115	39

TABLE 3
Sensitivity
(Source impedance = 270Ω)

Supply voltage (V)	Load (Ω)	Output power (W)	Nominal input current (r.m.s.) (mA)
24	3·75	40	14·3*
	5	34	13·5
	7·5	26	13·7
	15	15	13·7
28	3·75	56	16·2

*With low-limit output and driver transistors the input requirement with a 3·75Ω load for 40W and 24V is 17mA.

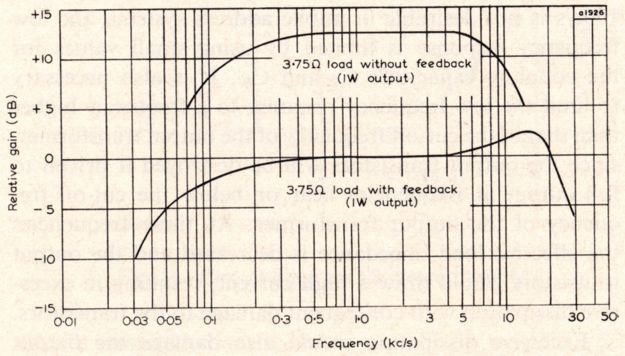


Fig. 8—Frequency response curves for 3·75Ω load at 1W level with or without feedback

However, if this control is situated at the input the signal-to-noise ratio may be unacceptable and for this reason the volume control is situated after the first stage as shown in Fig. 9. With the volume control in this position it is possible to mix the two inputs.

In the pick-up input stage the effects of spreads in the current amplification factor h_{fe} are reduced by application of local feedback. This feedback is applied by use of an undecoupled emitter resistor, which, in effect, determines the sensitivity of this stage since the amount of feedback depends on the value of the resistor. In the microphone input stage, the source impedance is low compared with the input impedance of the transistor which results in the effect of the current amplification factor spreads of the transistor being diminished.

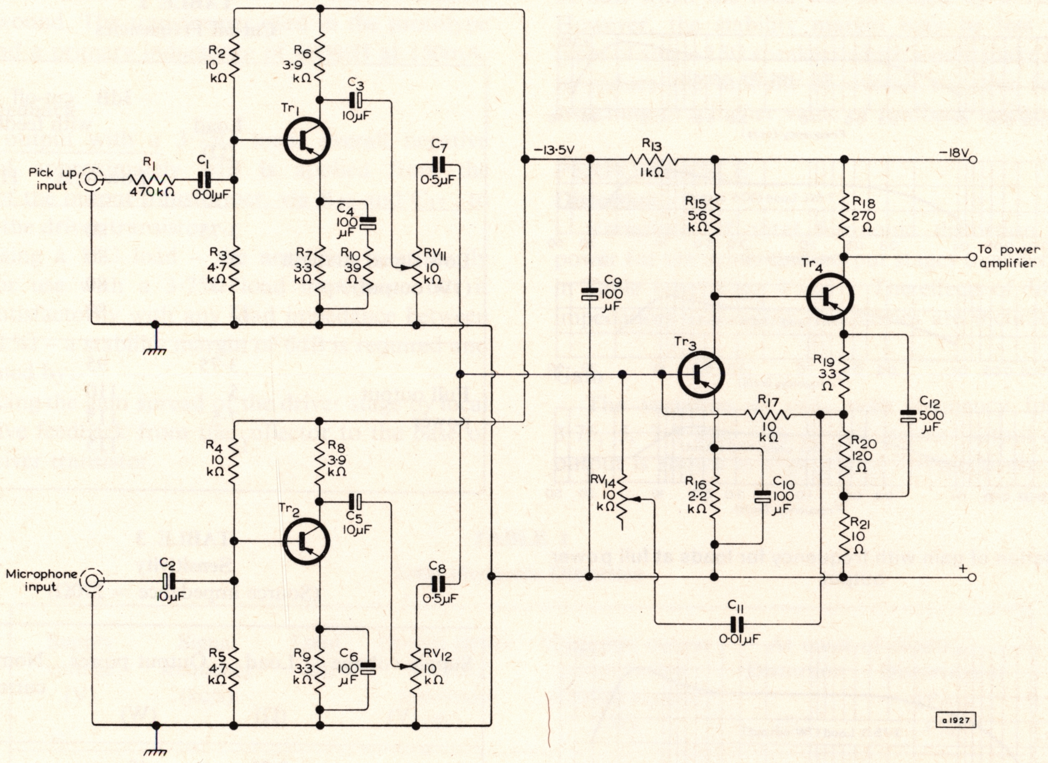


Fig. 9—Circuit diagram for pre-amplifier stage

As the reproduction of frequencies below about 150c/s is not desirable in public address systems, the low frequency response is limited by using small values for the coupling capacitors C_7 and C_8. It is also necessary to limit the low frequency response to a frequency higher than that of the cut-off frequency of the output transformer, since the output transistors will be destroyed if driven to full output at frequencies near or below the cut-off frequency of the output transformer. At these frequencies the effective load impedance is decreased and the output transistors would draw a high current, resulting in excessive dissipation with consequent damage to the transistors.

Excessive dissipation would also damage the output transistors if the output were short-circuited. Care should therefore be taken to avoid such an occurrence.

Second and Third Stages

The second and third stages are directly coupled and have d.c. feedback applied over them. This reduces the number of components used and improves d.c. stability. A.C. feedback is also applied over the second and third stages and its main purpose is to reduce gain spread.

For balanced reproduction it is desirable to limit the high frequency response and this is accomplished by incorporating a treble-cut control in the pre-amplifier.

PERFORMANCE OF PRE-AMPLIFIER

Sensitivity

The power amplifier needs approximately 15mA r.m.s. to give 40W output with 3·75Ω load. The pick-up input is 150mV (impedance 470kΩ) for 15mA r.m.s. output from the pre-amplifier. The microphone input (impedance 1·5kΩ approximately) is 1·3mV for 15mA r.m.s.

Gain

The variation of gain with frequency for the pre-amplifier and the effect of treble-cut control are illustrated in Fig. 10. Table 4 shows the −3dB cut-off frequencies for the pre-amplifier with minimum and maximum treble-cut control.

Signal-to-Noise Ratio

For the pick-up input, the signal-to-noise ratio is 53dB for an input of 150mV and an audio bandwidth of 20c/s to 20kc/s. For the microphone input, the signal-to-noise ratio is 60dB for an input of 1·3mV and an audio bandwidth of 20c/s to 20kc/s.

TABLE 4
Cut-off Frequencies of Pre-amplifier

Treble-cut control	−3dB cut-off frequencies	
	Low (c/s)	High (kc/s)
Minimum	120	>20
Maximum	100	2

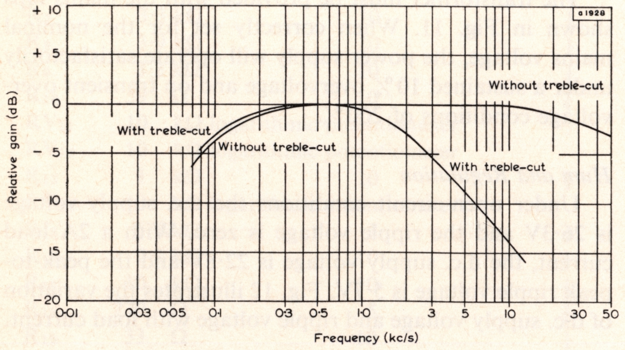


Fig. 10—Variation of gain with frequency and effect of treble-cut control for pre-amplifier

PERFORMANCE OF COMPLETE AMPLIFIER

Sensitivity

The pick-up input is 140mV (impedance 470kΩ) for full output power of 40W with 3·75Ω load. The microphone input is 1·2mV for full output power of 40W with 3·75Ω load.

Frequency Response

Table 5 shows the frequency response of the amplifier to treble-cut control.

TABLE 5
Frequency Response of Complete Amplifier

Load (Ω)	Frequency Response	
	Minimum treble-cut control	Maximum treble-cut control
3·75	120c/s to 18kc/s	100c/s to 2kc/s
5	120c/s to 20kc/s	110c/s to 2kc/s
7·5	120c/s to >20kc/s	115c/s to 2kc/s
15	120c/s to >20kc/s	115c/s to 2kc/s

Power Supply Requirements

The quiescent current with 24V supply is 290mA (the voltage of the power supply should not exceed 28V when providing the quiescent current). The current consumption for full sine-wave drive (40W output power with 3·75Ω load) is 3·1A. The current consumption for full drive, speech and music is 1·2A.

The amplifier is designed for operation from a nominal supply of 24V. A suitable supply for speech and music output would be two 12V accumulators in series. For operation from a.c. mains, a suitable supply for speech and music output would be the power supply described below.

D.C. CONDITIONS FOR 24V SUPPLY

Table 6 should be used in conjunction with the circuits shown in Figs. 1 and 9. The collector current of Tr_5 is 120mA and the total quiescent collector current of Tr_6 and Tr_7 is 60mA.

TABLE 6
D.C. Conditions

Point of Measurement		Voltage (V)
	C_{16}	−21
	C_{13}	−18
	C_9	−13·5
Tr_1	Emitter	−4·4
	Collector	−7·8
Tr_2	Emitter	−3·9
	Collector	−9·0
Tr_3	Emitter	−4·5
	Collector	−5·9
Tr_4	Emitter	−5·8
	Collector	−8·6
Tr_5	Emitter	−3·0
	Collector	−20·0

POWER SUPPLY

The circuit diagram of the power supply for the amplifier is given in Fig. 11. The regulation and ripple voltage are such that the power supply is suitable for speech and music operation. A more elaborate circuit is needed if the full output is required with sine-wave drive.

The power supply comprises a mains transformer, a full-wave rectification bridge consisting of four AY100 germanium rectifiers and a reservoir capacitor.

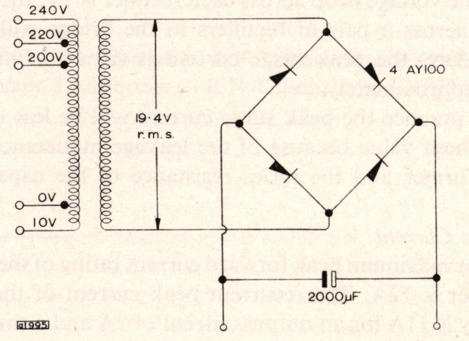


Fig. 11—Circuit diagram for power supply

Circuit Description

Referring to Fig. 11, mains taps are provided on the primary of the mains transformer to allow the power supply to operate at the nominal mains voltage. The transformer has a turns ratio of 11·85 : 1 and its secondary is connected to a bridge arrangement of four AY100 germanium rectifiers. The d.c. output of the bridge is connected across a 2000µF reservoir capacitor. On open circuit, the power supply has a nominal d.c. output voltage of approximately 26V and the ripple voltage is zero. When a load current of 2A is drawn, the d.c. output voltage decreases to 22V and the ripple voltage is then approximately 6V.

Design Considerations

Full-wave rectification is desirable in a power supply to achieve good regulation and low hum. This rectification can be obtained either by using two rectifiers in conjunction with a centre-tapped transformer or by using four rectifiers arranged as a bridge with a transformer which has a single secondary winding. The four rectifiers and the transformer with a single secondary winding were used since these cost less than the centre-tapped transformer and two rectifiers.

For full-wave rectification, the maximum value of the reservoir capacitor is limited to 2000µF by the recurrent peak current rating of the rectifiers.

Surge Current

The maximum surge current for the AY100 germanium rectifier is rated at 90A. This particular power supply has a maximum surge current of 70A and is thus well within the rating. The surge current is equal to the peak secondary open-circuit voltage of the transformer, less the voltage drop across the rectifiers, divided by the d.c. resistance referred to the secondary of the transformer.

The transformer used in the prototype power supply had a primary resistance of 22Ω, and a secondary resistance of 0·2Ω, and an r.m.s. secondary open-circuit voltage of 19·4V. The turns ratio of the transformer is therefore 230/19·4 or 11·85 when the transformer is used with a nominal mains voltage of 230V. The reflected primary resistance is thus $22/(11{\cdot}85)^2$ or 0·17Ω so that the total d.c. resistance referred to the secondary is 0·37Ω. Since the r.m.s. secondary open-circuit voltage is 19·4V, the peak secondary open-circuit voltage is 27·4V. If it is assumed that the voltage drop across each rectifier is 1V, the voltage drop across a pair of rectifiers in the bridge will be 2V. Therefore, the peak surge current is (27·4−2·0)/0·37, or 70A approximately.

In practice the peak surge current will be less than the calculated value because of the leakage inductance of the transformer and the series resistance of the capacitor.

Ripple Current

The maximum peak forward current rating of the AY100 rectifier is 12A. The recurrent peak current of the power supply is 11A for an output current of 2A and a smoothing capacitor of 2000µF.

Heat Sinks

Each heat sink is made of blackened 16 s.w.g. aluminium and has an area of 80cm^2. The heat sinks easily meet the normal operational requirements of the rectifiers.

Peak Voltage

The maximum peak inverse voltage rating of the AY100 rectifier is 120V. When the rectifier is connected into the bridge configuration of the power supply, it is subjected to a maximum peak inverse voltage of 28V at the nominal mains voltage. Thus the maximum peak inverse voltage rating of the AY100 rectifier is ample for any mains overvoltage or surge conditions which may occur.

Mains Taps

The transformer must be provided with the mains taps shown in Fig. 11. When correctly set for the nominal mains voltage, the power supply will operate satisfactorily under a sustained 10% overvoltage and on transient overvoltage conditions of 200%.

Hum and Regulation

Under open-circuit conditions the d.c. supply voltage is 26·3V and the ripple voltage is zero. With a 2A load current, the d.c. supply voltage is 22·8V and the peak-to-peak ripple voltage is 5·7V. Fig. 12 illustrates the variation of d.c. supply voltage and ripple voltage with load current.

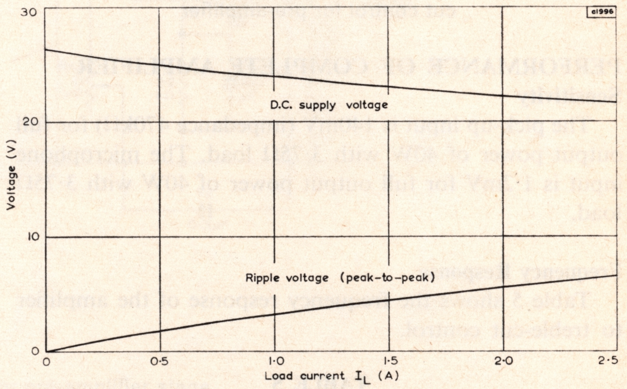


Fig. 12—Variation of d.c. supply voltage and ripple voltage with load current

Operation of Power Supply with Amplifier

The current consumption of the 40W transistor amplifier for full output with speech and music operation is about 1·2A, and the quiescent current consumption is 290mA. The peak-to-peak ripple voltages for these two conditions are 3·8 and 0·5V respectively. At the nominal input voltage, the corresponding d.c. supply voltages are 23·6 and 25·6V respectively. The peak output power with speech and music will vary between 34 and 44W (equivalent sine-wave output power levels) depending on the duration of the peak levels. A rise of 10% in the mains voltage will not damage the amplifier. For speech and music operation of the amplifier, the regulation of the power supply is satisfactory and the amount of hum is found to be generally acceptable.

If full output power of the amplifier is required with sine-wave drive, it will be necessary to provide a more elaborate power supply which should have better regulation and less hum.

LIST OF COMPONENTS

Pre-amplifier

Resistors

Circuit ref.	Value	Tolerance (± %)	Rating (W)
R_1	470 kΩ	10	$\frac{1}{4}$
R_2	10 kΩ	10	$\frac{1}{4}$
R_3	4·7 kΩ	10	$\frac{1}{4}$
R_4	10 kΩ	10	$\frac{1}{4}$
R_5	4·7 kΩ	10	$\frac{1}{4}$
R_6	3·9 kΩ	10	$\frac{1}{4}$
R_7	3·3 kΩ	10	$\frac{1}{4}$
R_8	3·9 kΩ	10	$\frac{1}{4}$
R_9	3·3 kΩ	10	$\frac{1}{4}$
R_{10}	39 Ω	10	$\frac{1}{4}$
RV_{11}	10 kΩ logarithmic potentiometer		
RV_{12}	10 kΩ logarithmic potentiometer		
R_{13}	1 kΩ	10	$\frac{1}{4}$
RV_{14}	10 kΩ logarithmic potentiometer		
R_{15}	5·6 kΩ	5	$\frac{1}{4}$
R_{16}	2·2 kΩ	10	$\frac{1}{4}$
R_{17}	10 kΩ	10	$\frac{1}{4}$
R_{18}	270 Ω	5	$\frac{1}{4}$
R_{19}	33 Ω	10	$\frac{1}{4}$
R_{20}	120 Ω	5	$\frac{1}{4}$
R_{21}	10 Ω	10	$\frac{1}{4}$

Capacitors

Circuit ref.	Value	Description	Rating (V)
C_1	0·01 µF	paper	
C_2	10 µF	electrolytic	16
C_3	10 µF	electrolytic	16
C_4	100 µF	electrolytic	16
C_5	10 µF	electrolytic	16
C_6	100 µF	electrolytic	16
C_7	0·5 µF	paper	
C_8	0·5 µF	paper	
C_9	100 µF	electrolytic	16
C_{10}	100 µF	electrolytic	16
C_{11}	0·01 µF	paper	
C_{12}	500 µF	electrolytic	12

Transistors

Ref.	Type
Tr_1 Tr_2 Tr_3	Mullard type AC107
Tr_4	Mullard type OC81

Power Amplifier

Resistors

Circuit ref.	Value	Tolerance (± %)	Rating (W)
R_{22}	68 Ω	10	$\frac{1}{4}$
R_{23}	2·2 kΩ	10	$\frac{1}{4}$
R_{24}	3·9 kΩ	10	$\frac{1}{4}$
R_{25}	330 Ω	10	$\frac{1}{4}$
R_{26}	22 Ω	10	$\frac{1}{4}$
RV_{27}	500 Ω pre-set potentiometer		
R_{28}	680 Ω	10	$\frac{1}{2}$
R_{29}	Mullard thermistor, type VA1053; 8Ω at 25°C		
R_{30}	8·2 Ω	10	$\frac{1}{4}$
R_{31}	Mullard thermistor, type VA1053; 8Ω at 25°C		
R_{32}	8·2 Ω	10	$\frac{1}{4}$
R_{33}	1 Ω	5	3·0
R_{34}	1 Ω	5	3·0
R_{35}	18 Ω	10	1·0
R_{36}	1·2 kΩ	10	$\frac{1}{4}$

Capacitors

Circuit ref.	Value	Description	Rating (V)
C_{13}	100 µF	electrolytic	25
C_{14}	100 µF	electrolytic	16
C_{15}	250 µF	electrolytic	25
C_{16}	1000 µF	electrolytic	25
C_{17}	2700 pF	silvered mica	

Transistors

Ref.	Type
Tr_5 Tr_6 Tr_7	Mullard type OC28

Transformers

Output Transformer — R.F. Gilson, Type EXP98B
Driver Transformer — R.F. Gilson, Type EXP98A

Transistorised 4W Transmitter for 8·315Mc/s

A. E. HILLING
Mullard Semiconductor Measurement and Application Laboratory

A 4W transmitter with economical power requirements is described for operation in the 8·3Mc/s region. Design procedure is based on the y parameters of the Mullard AUY10 transistor. For operation at the international 8·364Mc/s distress frequency, a crystal-controlled oscillator stage could be used. This can be replaced by a grounded-base feedback oscillator for general telegraphic use.

The design procedure is suitable for transistorised transmitters operating at other frequencies between 2 and 10Mc/s and at higher powers.

INTRODUCTION

The Mullard AUY10 is a germanium alloy-diffused transistor with maximum current and voltage ratings of 700mA and 60V respectively. The typical f_1 of 120Mc/s (at 300mA) makes this transistor suitable for medium power r.f. amplifiers (Ref. 1), and it has been used in a low-voltage low-battery-drain transmitter working at a frequency close to the International Marine Distress frequency of 8·364Mc/s (specified in Ref. 2).

Class B or Class C stages are necessary to give the required circuit operating efficiency, the supply voltage being either 12V or 24V.

The output power required of such a circuit depends to some extent on the permissible battery drain. In the present example a design figure of 4W is taken, this being an accepted value for distress applications. The efficiency of the AUY10 decreases appreciably at higher powers.

GENERAL DESIGN PROCEDURE

The output requirement of this transmitter is 4W into a 50Ω aerial at a frequency of 8·315Mc/s.

A suitable layout consists of an oscillator stage and a buffer amplifier (both small-signal class A stages) driving a single-ended driver amplifier and a push-pull output stage (both working in class B). Mullard OC170 transistors are used in the small-signal stages. The AUY10 is used in the driver and output stages.

Class B operation has been chosen in preference to class C, as the theoretical improvement in efficiency in class C has not been confirmed in practice. The discrepancy can be attributed to the phenomena of hole storage observed in this transistor, resulting in an increase of conduction angle.

Class A_1 modulation may be applied in the driver stage, or class A_2 in the driver and buffer stages. Low-level modulation may be used, as there is no requirement for speech modulation.

The push-pull output stage is designed first, from considerations of r.f. output power and supply voltage. A supply voltage of 24V is used because of the high effective knee voltage of the AUY10. These requirements determine the load which must be applied to the collectors of the transistors.

Small-signal y parameters are used to calculate the input admittance and power gain of the output stage. The use of small-signal parameters may be justified if they do not vary appreciably with collector current and voltage.

The driver stage is similarly designed, thereby determining the operating point of the buffer stage and the power requirement of the oscillator.

Two oscillator circuits are considered: one, a crystal-stabilised circuit for the distress application; the other, a feedback circuit for general purpose applications.

No frequency multiplication is employed in the transmitter.

The stages are discussed with reference to theoretical circuit diagrams. Component values quoted are those used in the practical circuit (Fig. 8) on page 62.

PUSH-PULL OUTPUT STAGE

A suitable output circuit is shown in Fig. 1. It is a conventional class B push-pull stage with the transistors in common emitter. However, as the collector of the AUY10 is connected directly to the case, this is bolted directly on to a heatsink (without insulation) to ensure good thermal transfer. It is considered preferable to have this heatsink at earth potential. The load is therefore transferred to the positive side of the h.t. supply, requiring a transformer input to this stage with isolated secondary windings.

Undecoupled emitter resistors of 1Ω are used to reduce the effect of transistor spreads and to minimise the effects of hole storage currents. No forward bias is applied to overcome cross-over distortion, as the output circuit is tuned.

The design output power is 4W. The efficiency of the output (aerial matching) circuit depends on realisable values of unloaded and working Q (respectively Q_o and Q_w) in this circuit.

The efficiency (η) of the circuit is given by

$$\eta = \left(1 - \frac{Q_w}{Q_o}\right)^2. \qquad \ldots(1)$$

An air-cored coil can be constructed with a Q_o of 200; and a Q_w of 10 is a reasonable compromise between harmonic rejection and power transfer. So that

$$\eta = \left(1 - \frac{10}{200}\right)^2 = 0{\cdot}9.$$

Therefore the power required from the output transistors is 4·4W. Allowing for the knee voltage of the AUY10 we may assume, with a 24V supply, a peak collector voltage swing (V_{cm}) of approximately 20V.

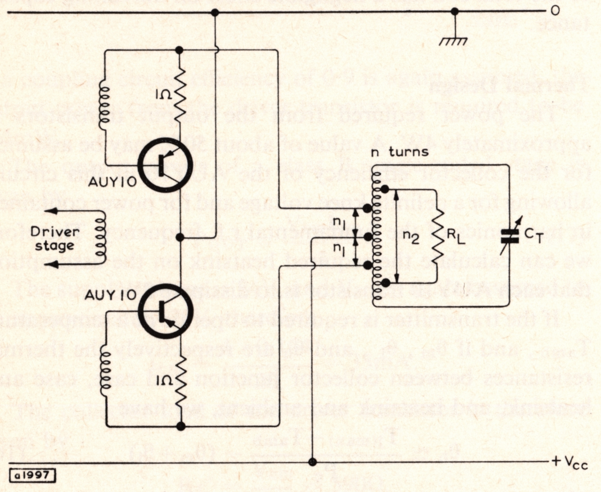


Fig 1—Output stage

The output power from a class B push-pull stage is given by

$$P_{out} = \frac{V_{cm} I_{cm}}{2}. \qquad \ldots(2)$$

The peak collector current excursion is therefore

$$I_{cm} = \frac{2 \times 4{\cdot}4}{20}\text{A} = 440\text{mA}.$$

The average battery consumption attributable to the output stage is therefore

$$I_{av} = \frac{2}{\pi} I_{cm} = 280\text{mA}.$$

For the required output power, the aerial load (R_L) must be reflected to the collectors of the output transistors as a resistance R_L' given by

$$R_L' = \frac{V_{cm}}{I_{cm}} = 46\Omega.$$

Little error is introduced if the output transformer is made nominally 1:1 for a 50Ω load.

Transistor y Parameters

The design and performance of the output stage are dependent on the transistor parameters. At 8Mc/s the y-parameter equivalent circuit is the most appropriate. Strictly, the large-signal y parameters should be used; but, owing to the difficulties of measurement, the small-signal values have been used at a nominal operating condition ($I_c = 220$mA, $V_{CE} = -12$V) which roughly corresponds to an instantaneous point $I_c = \frac{1}{2}.I_{cm}$, $V_{CE} = \frac{1}{2}.V_{cm}$. This selection of operating conditions is justified if the y parameters do not vary rapidly with I_c and V_{CE}.

The measured values of the y parameters for the AUY10 in common emitter at 8Mc/s are

$y_{ie} = 50+19j$ mmho $\qquad y_{oe} = 10+6j$ mmho
$y_{fe} = 100-325j$ mmho $\qquad y_{re} = -0{\cdot}4-3j$ mmho

Modification of Transistor y Parameters by Emitter Resistors

It may be shown that the insertion of a load in the emitter circuit modifies the effective transistor y parameters. The circuit Y parameters (that is, including the emitter resistor) have therefore been calculated from the transistor y parameters and the value of emitter resistance.

The circuit Y parameters are:

$$Y_{ie} = \frac{y_{ie}Y_e - \Delta y}{\Sigma y} \qquad \ldots(3)$$

$$Y_{fe} = \frac{y_{fe}Y_e + \Delta y}{\Sigma y} \qquad \ldots(4)$$

$$Y_{oe} = \frac{y_{oe}Y_e - \Delta y}{\Sigma y} \qquad \ldots(5)$$

$$Y_{re} = \frac{y_{re}Y_e + \Delta y}{\Sigma y} \qquad \ldots(6)$$

where

Y_e = external admittance of emitter circuit
$\Delta y = y_{fe}y_{re} - y_{oe}y_{ie}$
$\Sigma y = y_{ie} + y_{oe} + y_{fe} + y_{re} + Y_e$.

The derivations of the Y parameters are given in the Appendix (page 63). If the values of y parameters already given are inserted and Y_e is taken as 1000mmho (emitter resistor = 1Ω), the modified Y parameters become

$Y_{ie} = 37+27j$ mmho $\qquad Y_{oe} = 7+8j$ mmho
$Y_{fe} = 150-244j$ mmho $\qquad Y_{re} = -0{\cdot}7-3{\cdot}3j$ mmho.

Calculation of Input Admittance

The input admittance, Y_{IN}, of an amplifier working into a load admittance Y_L is given (Ref. 3) by

$$Y_{IN} = Y_{ie} - \frac{Y_{fe}Y_{re}}{Y_{oe}+Y_L}. \qquad \ldots(7)$$

For a transistor used at a frequency well below the cut-off frequency it may be assumed that, when the transistor is driven from a finite source admittance, the output admittance

$$Y_{OUT} \simeq Y_{oe}. \qquad \ldots(8)$$

Further, for a tuned amplifier,

$$B_L = -B_{OUT} \qquad \ldots(9)$$

where B_L and B_{OUT} are the susceptive components of Y_L and Y_{OUT}. Therefore

$$B_L \simeq -B_{oe} \qquad \ldots(10)$$

and

$$G_{oe}+G_L \gg B_{oe}+B_L. \qquad \ldots(11)$$

Therefore

$$Y_{IN} \simeq Y_{ie} - \frac{Y_{fe}Y_{re}}{G_{oe}+G_L} \qquad \ldots(12)$$

where G_{oe} and G_L are the conductive components of Y_{oe} and Y_L.

With $Y_L = 20$mmho ($R_L = 50\Omega$), and the values of Y parameters already given,

$$Y_{IN} = (37+27j) - \frac{(150-244j)(-0{\cdot}7-3{\cdot}3j)}{7+20}$$
$$= 71+39j \text{ mmho}.$$

Calculation of Power Gain

It may be shown (Ref. 3) that, for a tuned amplifier, the power gain is given by

$$\text{power gain} = \left|\frac{Y_{fe}}{G_{oe}+G_L}\right|^2 \frac{G_L}{G_{IN}}. \qquad \ldots(13)$$

Thus we have

$$\text{power gain} = \left|\frac{150-244j}{7+20}\right|^2 \frac{20}{71} = 30 \text{ (or 14·8dB)}.$$

The required output power of the driver stage is therefore 147mW.

Output Circuit Design

An air-cored transformer is used for coupling the output transistors to the load (Fig. 1).

Now

$$Q_w = \frac{1}{G_T \omega L} \qquad \ldots(14)$$

where

L = inductance of coil

$\omega = 2\pi \times$ operating frequency (8·315Mc/s)

and

G_T = total conductance across coil

given by

$$G_T = G_{OUT}\left(\frac{n_1}{n}\right)^2 + G_c + G_L\left(\frac{n_2}{n}\right)^2 \qquad \ldots(15)$$

where

$$G_{OUT} \simeq G_{oe}$$

G_c = coil loss conductance $= \dfrac{1}{Q_o \omega L}$ *

n_1, n_2, n = the number of primary, secondary, and total turns.

The transformer can be assumed to be an auto-transformer. In practice it may be convenient to earth one side of the load, thus necessitating an isolated secondary winding.

The value of Q_w has already been chosen (page 57), so that we have

$$Q_w = 10 = \frac{1}{52\times10^6 \times L \times 10^{-3}\left[7\left(\frac{n_1}{n}\right)^2 + 20\left(\frac{n_2}{n}\right)^2\right]}.$$

But $n_1 = n_2$ (page 57), therefore

$$L\left(\frac{n_1}{n}\right)^2 = \frac{1}{10\times52\times10^6\times10^{-3}\times27}.$$

The value of L may be determined by reference to a convenient value of tuning capacitance; 300pF is a suitable value, and it resonates with 1·5μH at 8·315Mc/s.

The value of n may be determined by examining the design of a practical coil (Ref. 4). For example, a coil of the following dimensions, wound with 14 s.w.g. silver-plated copper wire, has an inductance of 1·5μH.

Average diameter = 2cm
Winding length = 5·8cm
Total turns (n) = 15

We then have

$$n_1^2 = \frac{15^2}{1{\cdot}5\times10^{-6}\times10\times52\times10^6\times10^{-3}\times27}$$

so that

$$n_1 = 3{\cdot}3 = n_2.$$

The experimental optimum values of n_1 and n_2 were found to be 3·5 and 4 respectively.

The Q_o was approximately 200, so that

$$G_c = \frac{1}{200\times52\times1{\cdot}5} = 0{\cdot}06\text{mmho},$$

and the assumption that $G_c \ll G_T$ is justified.

The output capacitance of the transistors when referred to the total coil has a negligible effect on the tuning capacitance.

Thermal Design

The power required from the output transistors is approximately 4W. A value of about 50% may be assumed for the collector efficiency of the AUY10 in this circuit, allowing for a definite knee voltage and for power contained in harmonics of the fundamental r.f. frequency. Therefore we can calculate the required heatsink on the assumption that each AUY10 transistor is to dissipate 2W.

If the transmitter is required to operate at a temperature T_{amb}, and if θ_m, θ_i, and θ_h are respectively the thermal resistances between collector junction and case, case and heatsink, and heatsink and ambient, we have

$$\theta_h \simeq \frac{T_{j(max)} - T_{amb}}{P_c} - (\theta_m + \theta_i) \qquad \ldots(16)$$

where

$T_{j(max)}$ = maximum permissible continuous junction temperature

P_c = the power dissipated in the collector junction

and the small correction for the power dissipated in the emitter-base diodes is ignored.

An ambient temperature of 45°C may be taken as the highest value for this application.

For the AUY10, $T_{j(max)} = 75°\text{C}$, $\theta_m = 5{\cdot}5$degC/W, and (if the transistor is bolted to the heatsink via a metal washer) $\theta_i = 0{\cdot}2$degC/W.

For $P_c = 2\text{W}$ we have

$$\theta_h = \frac{75-45}{2} - (5{\cdot}5 - 0{\cdot}2) \simeq 8\text{degC/W}.$$

If the output transistors are bolted on to a 9in×9in cadmium-plated steel box which has a thermal resistance of approximately 4degC/W, the transistors are working below their maximum junction temperature at an ambient temperature of 45°C.

At $T_{j(max)}$ the collector leakage current I_{CBO} with zero emitter current is less than 4·5mA for a collector voltage of 60V. The change of I_{CBO} with junction temperature is less than 0·2mA/degC. It is easily calculated that, for the conditions defined above, the thermal stability factor of >10 is sufficiently great to prevent thermal runaway.

DRIVER STAGE

The circuit used in this stage is shown in Fig. 2. Here, as in the output stage, the AUY10 transistor is operated in common emitter, class B, with the collector and case at earth potential. A 1Ω emitter resistor is again used.

The power required to drive the output stage is 147mW, the input conductance of the output stage being 71mmho.

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*This term is negligible compared to the other components of G_T

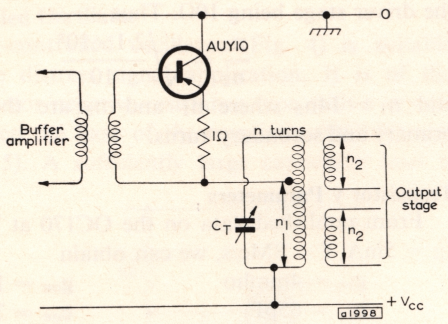

Fig. 2—Driver stage

If a coupling circuit efficiency of 0·9 is again assumed, the output power from the driver transistor is required to be 164mW.

The output power of a class B single-ended stage is given by

$$P_{OUT} = \frac{V_{cm} I_{cm}}{4}. \qquad \ldots(17)$$

The supply voltage is 24V, and V_{cm} is again assumed to be approximately 20V, therefore

$$I_{cm} = \frac{4\times0{\cdot}164}{20} = 33\text{mA}.$$

The collector load of the driver transistor is therefore given by

$$R_L' = \frac{V_{cm}}{I_{cm}} = 590\Omega.$$

The average battery consumption attributable to the driver stage is therefore

$$I_{av} = \frac{1}{\pi} I_{cm} = 11\text{mA}.$$

As the driver stage conducts every other half-cycle, the tuned circuit between the driver and output stages selects only the fundamental component of this half-wave rectified sinewave of current and transmits it to the output stage.

By a Fourier analysis it can be shown that the fundamental component consists of a sinewave of peak value equal to one-half of the peak value of the half-wave rectified sinewave.

The input resistance of the output stage is 14Ω, and this must be transformed by the coupling network to a value given by

$$R_x = \frac{V_{cm}}{0{\cdot}5 I_{cm}} = 1180\Omega.$$

That is,

$$\frac{n_1}{n_2} = \sqrt{\frac{1180}{14}}$$

where n_1 and n_2 are the numbers of primary and secondary turns on the interstage transformer. Hence

$$n_1 = 9{\cdot}2 n_2.$$

Transistor y Parameters

The operating condition of the driver stage has been determined in a manner similar to that used for the output stage. The y parameters have been taken at a point $I_c = 17\text{mA}$, $V_{CE} = -12\text{V}$. They are:

$y_{ie} = 60+36j$ mmho $y_{oe} = 8+6j$ mmho
$y_{fe} = 80-210j$ mmho $y_{re} = -0{\cdot}4-3j$ mmho.

Modification of Transistor y Parameters by Emitter Resistors

The circuit Y parameters are calculated from Eqs (3), (4), (5) and (6), with $Y_E = 1000$ mmho. We have

$Y_{ie} = 47{\cdot}5+39j$ mmho $Y_{oe} = 7+6j$ mmho
$Y_{fe} = 94-167j$ mmho $Y_{re} = -0{\cdot}7-2{\cdot}7j$ mmho.

Calculation of Input Admittance

As we have seen, the input admittance is given by Eq (12):

$$Y_{IN} \simeq Y_{ie} - \frac{Y_{fe}Y_{re}}{G_{oe}+G_L}$$

where

$$G_L = \frac{1}{R_L'}.$$

Thus

$$Y_{IN} = 47{\cdot}5+39j - \frac{(94-167j)(-0{\cdot}7-217j)}{7+1{\cdot}7}$$
$$= 100+54j \text{ mmho}.$$

Calculation of Power Gain

The power gain is given by Eq (13). Thus

$$\text{power gain} = \left|\frac{Y_{fe}}{G_{oe}+G_L}\right|^2 \frac{G_L}{G_{IN}}$$
$$= \left|\frac{94-167j}{7+1{\cdot}7}\right|^2 \frac{1{\cdot}7}{100} = 9 \text{(or 9·6dB)}.$$

The input power required from the buffer stage is therefore 18mW.

Design of Output Circuit of Driver Stage

The design method is that given under *Output Circuit Design* (page 58).

An air-cored transformer is used, with an assumed Q_w of 10. In this case, from Eqs (14) and (15),

$$Q_w \simeq \frac{1}{\left[G_{OUT}\left(\frac{n_1}{n}\right)^2 + G_{IN}\left(\frac{n_2}{2}\right)^2\right]\omega L}. \qquad \ldots(18)$$

Inserting values already calculated, we have

$$10 \simeq \frac{1}{\left[7\left(\frac{n_1}{n}\right)^2 + 71\left(\frac{n_2}{n}\right)^2\right]52\times10^6 L\times10^{-3}}.$$

But, as already shown, $n_1 = 9{\cdot}2n_2$, therefore

$$L\left(\frac{n_1}{n}\right)^2 = \frac{1}{410\times10^4}.$$

It is convenient to use a coil similar to that already designed (page 58); that is, with $L = 1{\cdot}5\mu\text{H}$ and $n = 15$.

Substitution in the above equations gives

$n_1 = 6{\cdot}0$ $n_2 = 0{\cdot}7$

The experimental values of n_1 and n_2 were found to be 7 and 1 respectively.

It is seen that the required tuning capacitance C_T is given by

$$C_T = \frac{1}{\omega^2 L} - C_{OUT}\left(\frac{n_1}{n}\right)^2 - C_{IN}'\left(\frac{n_2}{n}\right)^2 \qquad \ldots(19)$$

where C_{IN}' is the input capacitance of the output stage. That is,

$$C_{IN}' = \frac{38\times10^{-3}\times10^{12}}{52\times10^6} = 750\text{pF}$$

C_{OUT} is assumed to be $\frac{B_{oe}}{\omega}$

C_T is calculated to be 237pF.

It should be noted that C_{OUT} is a small but not negligible component of the tuning capacitance in this circuit.

BUFFER STAGE

The circuit used in this stage is shown in Fig. 3. An OC170 transistor is employed in common emitter, working in class A. The input power required by the driver stage is 18mW into a resistance of 10Ω.

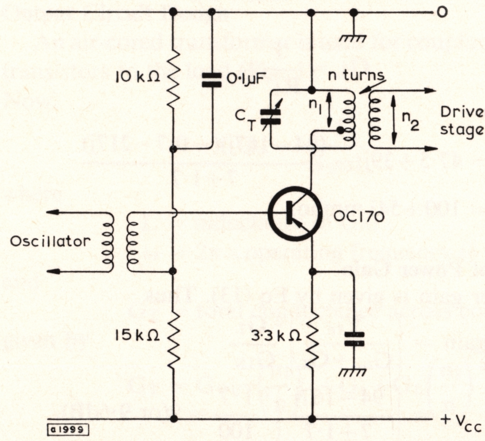

Fig. 3—Buffer amplifier

To give better harmonic rejection at this low level, a Q_w of 20 has been chosen for the interstage coupling network. An air-cored coil similar to those in the output and driver stages is used, giving a transformer efficiency of 0·81. The output power required from the buffer transistor is therefore 22mW.

The output power from a class A stage is

$$P_{OUT} = \frac{V_{cm}I_{cm}}{2}. \qquad \ldots(20)$$

To observe the 20V maximum collector voltage rating of the OC170 under maximum signal conditions it is necessary to restrict the d.c. operating collector voltage to 10V. With a 24V supply, 14V must be dropped external to the transistor; that is, across an emitter resistor. Allowing for a knee voltage of 0·5V, the available collector voltage swing is 9·5V; therefore

$$I_{cm} = 4·6\text{mA}.$$

The value of emitter resistor required is given by

$$R_e = \frac{14}{0·0046}\Omega = 3·2\text{k}\Omega.$$

A 3·3kΩ resistor can be used.

The d.c. bias conditions are defined by 10kΩ and 15kΩ resistors in the bias chain. The load, which consists of a tuned circuit, is placed in the collector.

The permitted collector dissipation of the OC170 is 50mW at 45°C ambient. This circuit is therefore toleranced for operation up to 45°C with 10% components and a supply voltage of 24V.

The collector load required is given by

$$R_L' = \frac{V_{cm}}{I_{cm}} = \frac{9·5}{4·6} = 2·1\text{k}\Omega.$$

The interstage coupling network must here again be used as an impedance transformer, the input resistance of the driver stage being 10Ω. Thus

$$\frac{n_1}{n_2} = \sqrt{\frac{2·1\times10^3}{10}}$$

and $n_1 = 14n_2$ where n_1 and n_2 are the numbers of primary and secondary turns.

Transistor y Parameters

From published data on the OC170 at $V_{CE} = -10$V, $I_E = 5$mA, f = 8Mc/s, we can obtain

$g_{ie} = 4$mmho　　$g_{oe} = 192\mu$mho
$c_{ie} = 65$pF　　$c_{oe} = 7$pF
$|y_{fe}| = 64$mA/V　　$|y_{re}| = 64\mu$mho
$\varnothing_{fe} = -30°$　　$\varnothing_{re} = 260°$.

Calculation of Input Admittance

The input admittance is given by Eq (12). Thus

$$Y_{IN} \simeq y_{ie} - \frac{y_{fe}y_{re}}{g_{oe}+G_L}$$

where

$$G_L = 1/R_L',$$

so that we have:

$$Y_{IN} = 4+3·4j - \frac{64\times0·064\angle230°}{0·19+0·47}$$
$$= 8·2+8·5j \text{ mmho}.$$

Calculation of Power Gain

The power gain is given by Eq (13). Thus

$$\text{power gain} = \left|\frac{y_{fe}}{g_{oe}+G_L}\right|^2 \frac{G_L}{G_{IN}}$$
$$= \left|\frac{64}{0·19+0·47}\right|^2 \frac{0·47}{8·2} = 350 \text{ (25dB)}.$$

Design of Output Circuit of Buffer Stage

The design method is again that given on page 58.

An air-cored transformer is used with an assumed Q_w of 20. In this case, inserting already calculated values into Eq (18), we have

$$20 \simeq \frac{1}{\left[0·19\left(\frac{n_1}{n}\right)^2+100\left(\frac{n_2}{n}\right)^2\right]52\times10^6\times10^{-3}L}.$$

But, as shown above, $n_1 = 14n_2$.

It is convenient to use a coil similar to those already designed; that is, with $L = 1·5\mu$H and $n = 15$.

Substitution in the above equation gives

$$n_1 = 14·5 \qquad n_2 = 1.$$

The experimental values of n_1 and n_2 were found to be 13·5 and 1 respectively. The required tuning capacitance C_T is given by Eq (19). Thus

$$C_T = \frac{1}{\omega^2L} - C_{OUT}\left(\frac{n_1}{n}\right)^2 - C_{IN}''\left(\frac{n_2}{n}\right)^2$$

where C_{IN}'' is the input capacitance of the driver stage. That is,

$$C_{IN}'' = 1000\text{pF}.$$

C_{OUT} is assumed to be $\frac{b_{oe}}{\omega}$

C_T is calculated to be 238pF.

OSCILLATOR

Alternative oscillator stages are described.

Crystal-controlled Oscillator

The crystal-controlled oscillator (Fig. 4) is suitable for use in the distress signal application. It is of the grounded-collector negative-resistance type with a crystal inserted between the base of the transistor (OC170) and ground (Ref. 5). A sufficiently large capacitive load is applied in the emitter lead. This gives an input impedance consisting of a negative resistance in parallel with a capacitance. An inductive impedance in the base will therefore cause the circuit to oscillate. In this case the inductance is provided by the crystal when it is operated just off parallel resonance. The direct current to the transistor is passed through an inductance in parallel with the capacitance in the emitter lead.

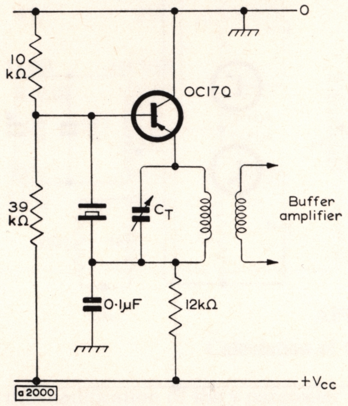

Fig. 4—Crystal-controlled oscillator

The d.c. bias conditions are determined by the 12kΩ resistor in the emitter and the 10kΩ and 39kΩ resistors in the bias chain. The transistor is biased at approximately $V_{CE} = -5$V, $I_E = 1·5$mA. The output power is approximately 0·1mW. The input to the buffer stage is taken via a loosely-coupled secondary winding from the inductance in the emitter.

Grounded-base Feedback Oscillator

This grounded-base feedback oscillator (Fig. 5) is suitable for general telegraphy applications. It uses an OC170 in grounded-base configuration, and it has external feedback applied between collector and emitter (Ref. 6). The bias conditions are defined by the 10kΩ and 4·7kΩ resistors in the bias chain and by the 1·8kΩ resistor in the emitter. The input to the buffer stage is taken via a secondary winding from the tuned circuit in the collector. The output power is approximately 0·1mW.

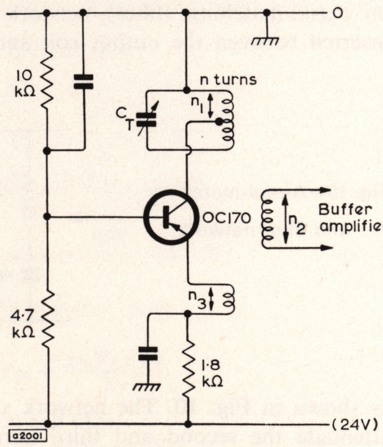

Fig. 5—Grounded-base feedback oscillator

In Fig. 5, $C_T \simeq 200$pF, n = 15 turns, $n_1 = 7\frac{1}{2}$ turns, $n_2 = 2$ turns, $n_3 = 2$ turns.

MODULATION

The transmitter has been designed to give an unmodulated r.f. output power of 4W (strictly speaking, class A_0 modulation). Class A_1 or A_2 modulation can be used.

For class A_1 modulation (keyed carrier) the circuit shown in Fig. 6 has been used. The insertion of a morse key interrupting the d.c. supply to the driver stage provides the means of interrupting the r.f. output. The r.f. choke and parallel capacitance are for interstage decoupling.

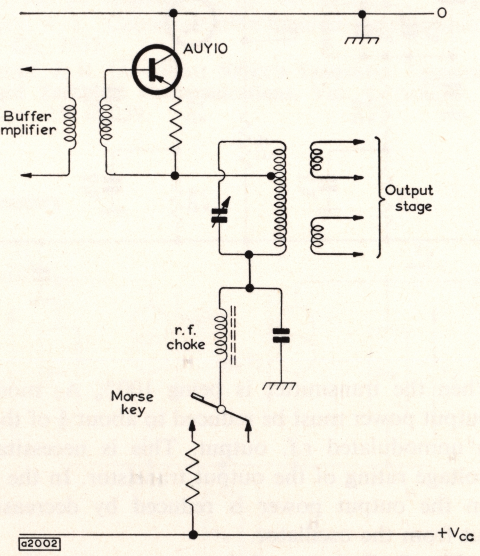

Fig. 6—Driver stage adapted for A_1 modulation

Class A_2 modulation (either keyed a.f. or keyed modulated emission) is applied via the base of the buffer stage (Fig. 7). For keyed a.f. modulation, the morse key is withdrawn from the driver stage, and the a.f. input to the base of the buffer stage is itself keyed. For keyed modulated emission, however, the morse key is retained in the driver stage, and continuous a.f. is injected into the base of the buffer stage.

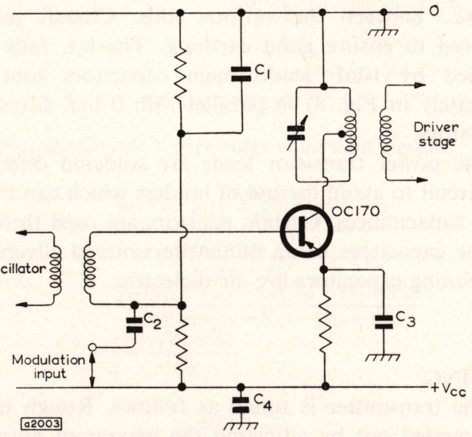

Fig. 7—Buffer amplifier adapted for A_2 modulation

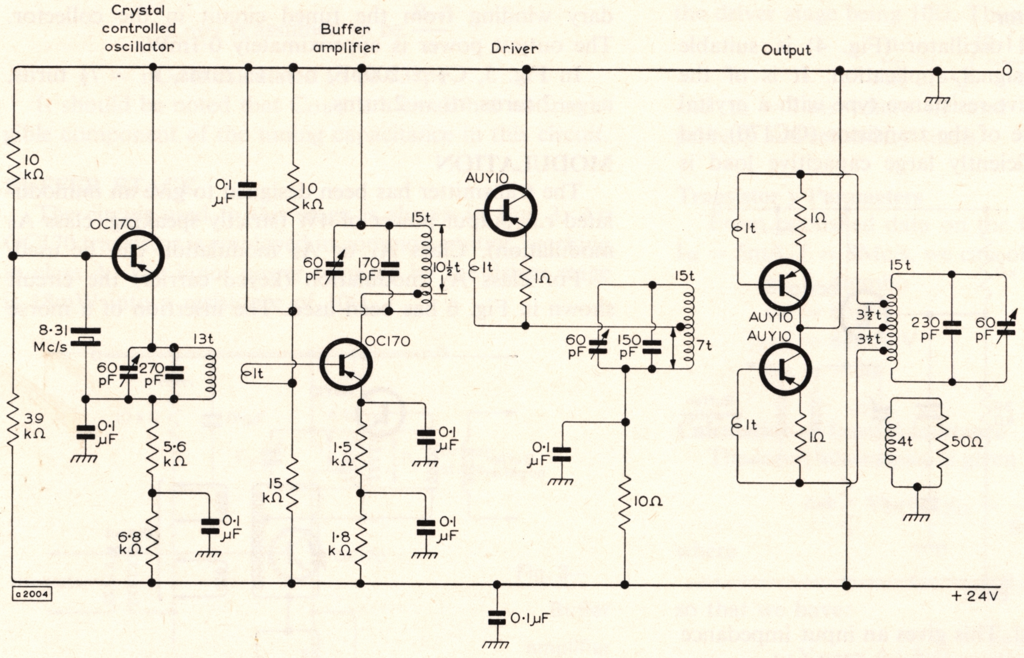

Fig. 8—Practical transmitter

When the transmitter is being 100% A_2 modulated, the output power must be reduced to about $\frac{3}{8}$ of the maximum unmodulated r.f. output. This is necessitated by the voltage rating of the output transistor. In the present design the output power is reduced by decreasing the output from the oscillator.

In Fig. 7, C_1 is an r.f. bypass capacitor, C_3 and C_4 bypass all frequencies, and C_2 is an a.f. bypass capacitor.

A_2 modulation up to 100% from 300c/s to 3kc/s can be obtained with this method.

CONSTRUCTION

A complete transmitter has been constructed according to the circuit in Fig. 8. This transmitter is built in a cadmium-plated steel box with screening of the same material between the various coils. Chassis joints are soldered to ensure good earthing. The h.t. rails are decoupled by 10nF leadthrough capacitors (not shown separately in Fig. 8) in parallel with 0·1μF silvered-mica capacitors.

The power transistor leads are soldered directly into the circuit to avoid the use of holders which can introduce stray capacitances. Carbon resistors are used throughout, all the capacitors being miniature sintered silvered-mica. The tuning capacitors are air dielectric.

TUNING

The transmitter is tuned as follows. Rough tuning is first carried out by adjusting the maximum output with a reduced drive voltage. This adjustment is obtained by displacing the loosely-coupled secondary winding of the oscillator output circuit. The signal is then increased until the collector current waveform shows a small dip (Fig. 9a) which is caused by the output transistor bottoming (the collector diode becomes forward-biased and returns some of the holes to the base, thereby reducing the collector current). The tuning is then adjusted until the dip appears at the peak of the waveform (Fig. 9b), the drive being then reduced until the dip disappears (Fig. 9c).

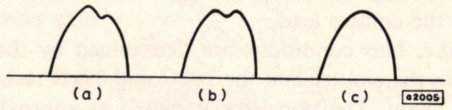

Fig. 9—Collector current waveforms observed during tuning

PERFORMANCE

The performance of the transmitter is summarised in Table 1, which shows results obtained with low-gain or high-gain AUY10 transistors in the driver and output stages.

The load was a 50Ω power meter; but for practical use an aerial-matching (filter) network would have to be inserted between the output coil and aerial (Refs. 7, 8), as shown in Fig. 10. The network shown is designed to attenuate the second and third harmonics: These were found to be more than 55dB down on the fundamental frequency.

Fig. 10—Aerial-matching and filter network

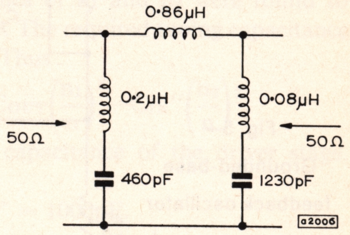

TABLE 1
Performance of Transmitter

	Low-gain AUY10	High-gain AUY10	
Room temperature	25°C	25°C	45°C
Output power	4W	5W	4·8W
Power gain			
output stage	14dB	15dB	—
driver stage	8·5dB	9dB	—
Efficiency			
output stage	40%	45%	35%
driver stage	33%	40%	—

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APPENDIX
Calculation of Circuit Y Parameters

Figs. 11 and 12 illustrate the modification of the y parameter equivalent circuit due to a load in the emitter. For the equivalence of the circuits,

$$Y_{ie} = \frac{I_1}{V_1'} \qquad Y_{oe} = \frac{I_2}{V_2'}$$

$$Y_{fe} = \frac{I_2}{V_1'} \qquad Y_{re} = \frac{I_1}{V_2'}$$

Expanding for $Y_{ie}Y_{fe}$, we have:

$$I_1+I_2+V_eY_e = 0 \qquad \text{...(A1)}$$

$$V_e = V_2 \qquad \text{...(A2)}$$

$$I_1 = y_{re}V_2+y_{ie}V_1 \qquad \text{...(A3)}$$

$$I_2 = y_{fe}V_1+y_{oe}V_2 \qquad \text{...(A4)}$$

$$V_1-V_e = V_1' \qquad \text{...(A5)}$$

$$\left(\text{where } Y_e = \frac{1}{R_e}\right)$$

whence from Eqs (A4) and (A5)

$$Y_{fe} = \frac{y_{fe}V_1+y_{oe}V_2}{V_1-V_e} \qquad \text{...(A6)}$$

and from Eq (A2)

$$= \frac{y_{fe}V_1+y_{oe}V_2}{V_1-V_2}.$$

Now, from Eqs (A1), (A3), and (A4)

$$y_{fe}V_1+y_{oe}V_2+y_{re}V_2+y_{ie}V_1+V_eY_e = 0$$

and therefore from Eq (A2)

$$V_1(y_{fe}+y_{ie}) = -V_2(y_{oe}+y_{re}+Y_e). \qquad \text{...(A7)}$$

Substituting (A7) in Eq (A6) gives

$$Y_{fe} = \frac{y_{fe}V_1-y_{oe}\left(\dfrac{y_{fe}+y_{ie}}{y_{oe}+y_{re}+Y_e}\right)V_1}{V_1+V_1\left(\dfrac{y_{fe}+y_{ie}}{y_{oe}+y_{re}+Y_e}\right)}$$

$$= \frac{y_{fe}Y_e+(y_{fe}y_{re}-y_{oe}y_{ie})}{y_{ie}+y_{re}+y_{fe}+y_{oe}+Y_e}.$$

If

$$\Sigma y = y_{ie}+y_{re}+y_{fe}+y_{oe}+Y_e$$

then

$$\Delta y = y_{fe}y_{re}-y_{oe}y_{ie}$$

so that

$$Y_{fe} = \frac{y_{fe}Y_e+\Delta y}{\Sigma y}.$$

Similarly, from Eqs (A3) and (A5)

$$Y_{ie} = \frac{y_{re}V_2+y_{ie}V_1}{V_1-V_e}. \qquad \text{...(A8)}$$

Substitution of (A7) in Eq (A8) gives

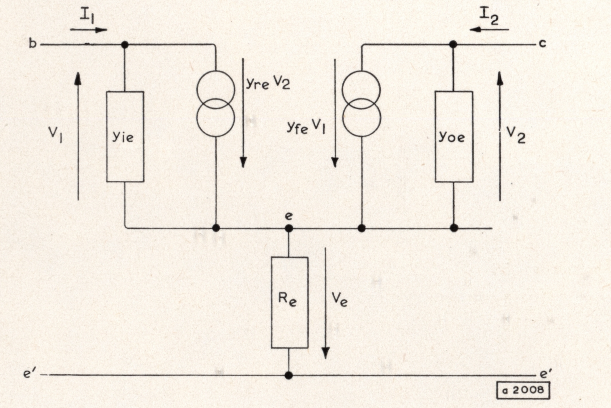

Fig. 11—Transistor y parameter equivalent circuit with emitter resistor

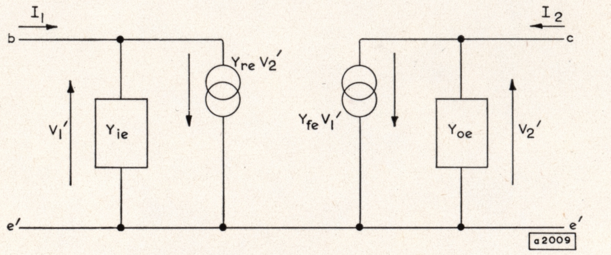

Fig. 12—Circuit Y parameter equivalent circuit

$$V_{ie} = \frac{y_{re}V_2-y_{ie}\left(\dfrac{y_{oe}+y_{re}+Y_e}{y_{fe}+y_{ie}}\right)V_2}{-V_2\left(\dfrac{y_{oe}+y_{re}+Y_e}{y_{fe}+y_{ie}}\right)-V_2}$$

$$= \frac{y_{re}(y_{fe}+y_{ie})-y_{ie}(y_{oe}+y_{re}+Y_e)}{-(y_{oe}+y_{re}+Y_e)-(y_{fe}+y_{ie})}$$

$$= \frac{-y_{ie}Y_e+\Delta y}{-\Sigma y}$$

so that

$$Y_{ie} = \frac{y_{ie}Y_e-\Delta y}{\Sigma y}.$$

Since the circuit of Fig. 12 is a symmetrical four-pole,

$$Y_{oe} = \frac{y_{oe}Y_e-\Delta y}{\Sigma y}$$

and

$$Y_{re} = \frac{y_{re}Y_e+\Delta y}{\Sigma y}.$$